



EEPROM-Programmable, Hex/Quad, Power-Supply Sequencers/Supervisors

General Description

The MAX6874/MAX6875 EEPROM-configurable, multi-voltage supply sequencers/supervisors monitor several voltage detector inputs and general-purpose logic inputs, and provide programmable open-drain outputs for highly configurable power-supply sequencing applications. The MAX6874 provides six voltage monitor inputs, four general-purpose inputs, and eight programmable open-drain outputs. The MAX6875 provides four voltage monitor inputs, three general-purpose inputs, and five programmable open-drain outputs. Manual reset and margin disable inputs provide additional flexibility.

All voltage detectors offer configurable thresholds for undervoltage detection. One high-voltage input (IN1) provides detector threshold voltages from +2.5V to +13.2V in 50mV increments, or from +1.25V to +7.625V in 25mV increments. A second positive input (IN2) provides detector threshold voltages from +2.5V to +5.5V in 50mV increments, or from +1.25V to +3.05V in 25mV increments. Positive inputs (IN3–IN6) provide detector threshold voltages from +1V to +5.5V in 20mV increments, or from +0.5V to +3.05V in 10mV increments.

Programmable output stages control power-supply sequencing or system resets/interrupts. Program the open-drain outputs as active-high or active-low. Programmable timing delay blocks configure each output to wait between 25 μ s and 1600ms before deasserting.

An SMBus™/I²C™-compatible serial data interface programs and communicates with the configuration EEPROM, the configuration registers, and the internal 4kb user EEPROM of the MAX6874/MAX6875.

The MAX6874/MAX6875 are available in a 7mm x 7mm x 0.8mm 32-pin thin QFN package and operate over the extended temperature range (-40°C to +85°C).

Applications

Telecommunications/Central Office Systems
Networking Systems
Servers/Workstations
Base Stations
Storage Equipment
Multimicroprocessor/Voltage Systems

Pin Configurations, Typical Operating Circuit, and Selector Guide appear at end of data sheet.

Features

- ◆ **Six (MAX6874) or Four (MAX6875) Configurable Input Voltage Detectors**
 - One High Voltage Input (+1.25V to +7.625V or +2.5V to +13.2V Thresholds)
 - One Voltage Input (+1.25V to +3.05V or +2.5V to +5.5V)
 - Four (MAX6874) or Two (MAX6875) Positive Voltage Inputs (+0.5V to +3.05V or +1V to +5.5V)
- ◆ **Four (MAX6874) or Three (MAX6875) General-Purpose Logic Inputs**
- ◆ **Two Configurable Watchdog Timers**
- ◆ **Eight (MAX6874) or Five (MAX6875) Programmable Open-Drain Outputs**
 - Active-High or Active-Low
 - Timing Delays from 25 μ s to 1600ms
- ◆ **Margining Disable and Manual Reset Controls**
- ◆ **4kb Internal User EEPROM**
 - Endurance: 100,000 Erase/Write Cycles
 - Data Retention: 10 Years
- ◆ **I²C/SMBus-Compatible Serial Configuration/Communication Interface**
- ◆ **±1% Threshold Accuracy**

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | PKG CODE |
|-------------|----------------|-------------|----------|
| MAX6874 ETJ | -40°C to +85°C | 32 Thin QFN | T3277-2 |
| MAX6875 ETJ | -40°C to +85°C | 32 Thin QFN | T3277-2 |

SMBus is a trademark of Intel Corp.

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ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND)
 IN2–IN6, ABP, SDA, SCL, A0, A1,
 GPI1–GPI4, MR, MARGIN, PO5–PO8
 (MAX6874), PO3–PO5 (MAX6875).....-0.3V to +6V
 IN1, PO1–PO4 (MAX6874), PO1–PO2 (MAX6875)....-0.3V to +14V
 DBP-0.3V to +3V
 Input/Output Current (all pins).....±20mA

Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)
 32-Pin 7mm x 7mm Thin QFN
 (derate 33.3mW/°C above +70°C).....2667mW
 Operating Temperature Range-40°C to +85°C
 Maximum Junction Temperature+150°C
 Storage Temperature Range.....-65°C to +150°C
 Lead Temperature (soldering, 10s).....+300°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{IN1} = +6.5\text{V}$ to +13.2V, V_{IN2} – $V_{IN6} = +2.7\text{V}$ to +5.5V, $GPI_ = \text{GND}$, $\overline{\text{MARGIN}} = \overline{\text{MR}} = \text{DBP}$, $T_A = -40^\circ\text{C}$ to +85°C, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------------------------------|--|------------------------------------|------|-------|------------|
| Operating Voltage Range (Note 3) | V_{IN1} | Voltage on IN1 to ensure the device is fully operational, IN3–IN6 = GND | 4.0 | | 13.2 | V |
| | V_{IN3} to V_{IN5} | Voltage on any one of IN3–IN5 to ensure the device is fully operational, IN1 = GND | 2.7 | | 5.5 | |
| IN1 Supply Voltage (Note 3) | V_{IN1P} | Minimum voltage on IN1 to guarantee that the device is powered through IN1 | | | 6.5 | V |
| Undervoltage Lockout | V_{UVLO} | Minimum voltage on one of IN3–IN5 to guarantee the device is EEPROM configured. | | | 2.5 | V |
| Supply Current | I_{CC} | $V_{IN1} = +13.2\text{V}$, IN2–IN6 = GND, no load | | 1.2 | 1.5 | mA |
| | | Writing to configuration registers or EEPROM, no load | | 1.3 | 2 | mA |
| Threshold Range | V_{TH} | V_{IN1} (50mV increments) | 2.5 | | 13.2 | V |
| | | V_{IN1} (25mV increments) | 1.250 | | 7.625 | |
| | | V_{IN2} (50mV increments) | 2.50 | | 5.5 | |
| | | V_{IN2} (25mV increments) | 1.250 | | 3.05 | |
| | | V_{IN3} – V_{IN6} (20mV increments) | 1.0 | | 5.5 | |
| | | V_{IN3} – V_{IN6} (10mV increments) | 0.50 | | 3.05 | |
| Threshold Accuracy | | IN1–IN6, $V_{IN_}$ falling | $T_A = +25^\circ\text{C}$ | -1.0 | +1.0 | % |
| | | | $T_A = -40^\circ\text{C}$ to +85°C | -1.5 | +1.5 | |
| Threshold Hysteresis | $V_{TH-HYST}$ | | | 0.3 | | % V_{TH} |
| Reset Threshold Temperature Coefficient | $\Delta V_{TH}/^\circ\text{C}$ | | | 10 | | ppm/ °C |
| Threshold-Voltage Differential Nonlinearity | $V_{TH DNL}$ | | -1 | | +1 | LSB |

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ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = +6.5V to +13.2V, V_{IN2} – V_{IN6} = +2.7V to +5.5V, GPI_{-} = GND, $MARGIN = \overline{MR} = DBP$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|--|------------------------|--|-----|-------|--------|-----------|-------|
| IN1 Input Leakage Current | I_{LIN1} | For $V_{IN1} <$ the highest of V_{IN3} – V_{IN5} | | 100 | 140 | μA | |
| IN2 Input Impedance | R_{IN2} | | 160 | 230 | 320 | $k\Omega$ | |
| IN3–IN6 Input Impedance | R_{IN3} to R_{IN6} | $V_{IN1} > 6.5V$ | 70 | 100 | 145 | $k\Omega$ | |
| Power-Up Delay | t_{PU} | $V_{ABP} \geq V_{UVLO}$ | | | 3.5 | ms | |
| IN_ to PO_ Delay | t_{DPO} | $V_{IN_}$ falling or rising, 100mV overdrive | | 25 | | μs | |
| PO_ Timeout Period | t_{RP} | Register contents (Table 16) | 000 | | 25 | μs | |
| | | | 001 | 1.406 | 1.5625 | | 1.719 |
| | | | 010 | 5.625 | 6.25 | | 6.875 |
| | | | 011 | 22.5 | 25 | | 27.5 |
| | | | 100 | 45 | 50 | | 55 |
| | | | 101 | 180 | 200 | | 220 |
| | | | 110 | 360 | 400 | | 440 |
| | | | 111 | 1440 | 1600 | | 1760 |
| PO1–PO4 (MAX6874), PO1–PO2 (MAX6875) Output Low (Note 3) | V_{OL} | $V_{ABP} \geq +2.5V$, $I_{SINK} = 500\mu A$ | | | 0.3 | V | |
| | | $V_{ABP} \geq +4.0V$, $I_{SINK} = 2mA$ | | | 0.4 | | |
| PO5–PO8 (MAX6874), PO3–PO5 (MAX6875) Output Low (Note 3) | V_{OL} | $V_{ABP} \geq +2.5V$, $I_{SINK} = 1mA$ | | | 0.3 | V | |
| | | $V_{ABP} \geq +4.0V$, $I_{SINK} = 4mA$ | | | 0.4 | | |
| PO1–PO8 Output Initial Pulldown Current | I_{PD} | $V_{ABP} \leq V_{UVLO}$, $V_{PO_} = 0.8V$ | | 10 | 40 | μA | |
| PO1–PO8 Output Open-Drain Leakage Current | I_{LKG} | Output high impedance | -1 | | +1 | μA | |

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ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = +6.5V to +13.2V, V_{IN2} – V_{IN6} = +2.7V to +5.5V, GPI_{-} = GND, $MARGIN = \overline{MR} = DBP$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|---|----------------|--|-----|-------|-------|--------|----|
| \overline{MR} , \overline{MARGIN} , GPI_{-} Input Voltage | V_{IL} | | | | 0.8 | V | |
| | V_{IH} | | 1.4 | | | | |
| \overline{MR} Input Pulse Width | t_{MR} | | 1 | | | μs | |
| \overline{MR} Glitch Rejection | | | | 100 | | ns | |
| \overline{MR} to PO_{-} Delay | t_{DMR} | | | 2 | | μs | |
| \overline{MR} to V_{DBP} Pullup Current | I_{MR} | $V_{\overline{MR}} = +1.4V$ | 5 | 10 | 15 | μA | |
| \overline{MARGIN} to V_{DBP} Pullup Current | I_{MARGIN} | $V_{\overline{MARGIN}} = +1.4V$ | 5 | 10 | 15 | μA | |
| GPI_{-} to PO_{-} Delay | $t_{DGPI_{-}}$ | | | 200 | | ns | |
| GPI_{-} Pulldown Current | $I_{GPI_{-}}$ | $V_{GPI_{-}} = +0.8V$ | 5 | 10 | 15 | μA | |
| Watchdog Input Pulse Width | t_{WDI} | GPI_{-} configured as a watchdog input | 50 | | | ns | |
| Watchdog Timeout Period | t_{WD} | Register Contents (Table 19) | 000 | 5.625 | 6.25 | 6.875 | ms |
| | | | 001 | 22.5 | 25 | 27.5 | |
| | | | 010 | 90 | 100 | 110 | |
| | | | 011 | 360 | 400 | 440 | |
| | | | 100 | 1.44 | 1.6 | 1.76 | s |
| | | | 101 | 5.76 | 6.4 | 7.04 | |
| | | | 110 | 23.04 | 25.6 | 28.16 | |
| | | | 111 | 92.16 | 102.4 | 112.64 | |
| SERIAL INTERFACE LOGIC (SDA, SCL, A0, A1) | | | | | | | |
| Logic-Input Low Voltage | V_{IL} | | | | 0.8 | V | |
| Logic-Input High Voltage | V_{IH} | | 2.0 | | | V | |
| Input Leakage Current | I_{LKG} | | -1 | | +1 | μA | |
| Output Voltage Low | V_{OL} | $I_{SINK} = 3mA$ | | | 0.4 | V | |
| Input/Output Capacitance | $C_{I/O}$ | | | 10 | | pF | |

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TIMING CHARACTERISTICS

(IN1 = GND, VIN2–VIN6 = +2.7V to +5.5V, GPI_ = GND, MARGIN = MR = DBP, TA = -40°C to +85°C, unless otherwise noted. Typical values are at TA = +25°C.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---------|--------------|-----|-----------------------|-----|-------|
| TIMING CHARACTERISTICS (Figure 2) | | | | | | |
| Serial Clock Frequency | fSCL | | | | 400 | kHz |
| Clock Low Period | tLOW | | 1.3 | | | μs |
| Clock High Period | tHIGH | | 0.6 | | | μs |
| Bus-Free Time | tBUF | | 1.3 | | | μs |
| START Setup Time | tSU:STA | | 0.6 | | | μs |
| START Hold Time | tHD:STA | | 0.6 | | | μs |
| STOP Setup Time | tSU:STO | | 0.6 | | | μs |
| Data-In Setup Time | tSU:DAT | | 100 | | | ns |
| Data-In Hold Time | tHD:DAT | | 0 | | 900 | ns |
| Receive SCL/SDA Minimum Rise Time | tR | (Note 4) | | 20 + 0.1 x CBUS | | ns |
| Receive SCL/SDA Maximum Rise Time | tR | (Note 4) | | 300 | | ns |
| Receive SCL/SDA Minimum Fall Time | tF | (Note 4) | | 20 + 0.1 x CBUS | | ns |
| Receive SCL/SDA Maximum Fall Time | tF | (Note 4) | | 300 | | ns |
| Transmit SDA Fall Time | tF | CBUS = 400pF | | 20 + 0.1 x CBUS | 300 | ns |
| Pulse Width of Spike Suppressed | tSP | (Note 5) | | 50 | | ns |
| EEPROM Byte Write Cycle Time | tWR | (Note 6) | | | 11 | ms |

Note 1: Specifications guaranteed for the stated global conditions. The device also meets the parameters specified when $0 < V_{IN1} < +6.5V$, and at least one of V_{IN3} – V_{IN6} is between +2.7V and +5.5V, while the remaining V_{IN3} – V_{IN6} are between 0 and +5.5V.

Note 2: Device may be supplied from any one of IN_, except IN2 and IN6.

Note 3: The internal supply voltage, measured at ABP, equals the maximum of IN3–IN5 if $V_{IN1} = 0$, or equals +5.4V if $V_{IN1} > +6.5V$. For $+4V < V_{IN1} < +6.5V$ and V_{IN3} – $V_{IN5} > +2.7V$, the input that powers the device cannot be determined.

Note 4: CBUS = total capacitance of one bus line in pF. Rise and fall times are measured between $0.1 \times V_{BUS}$ and $0.9 \times V_{BUS}$.

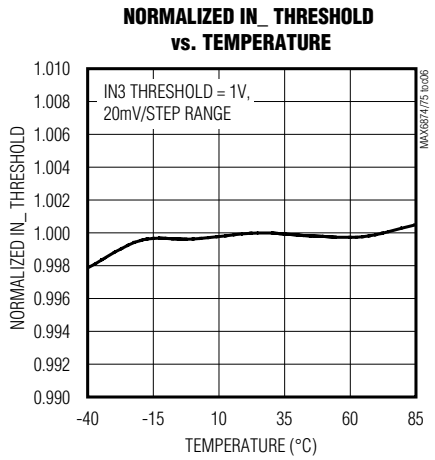
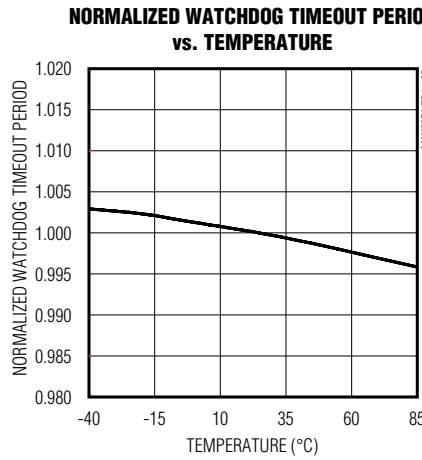
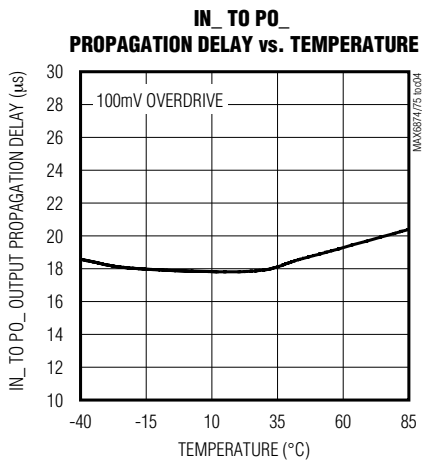
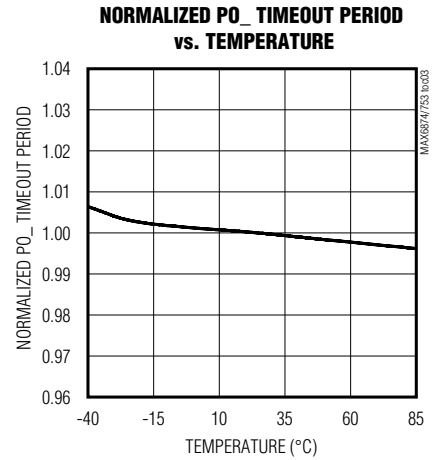
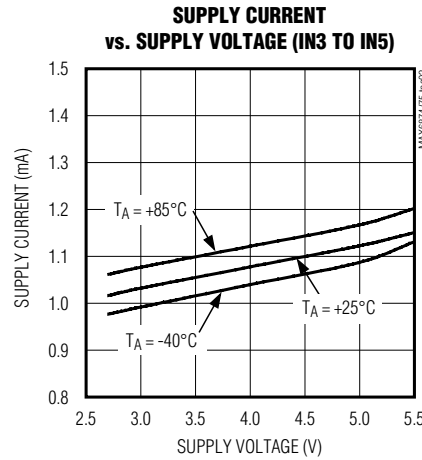
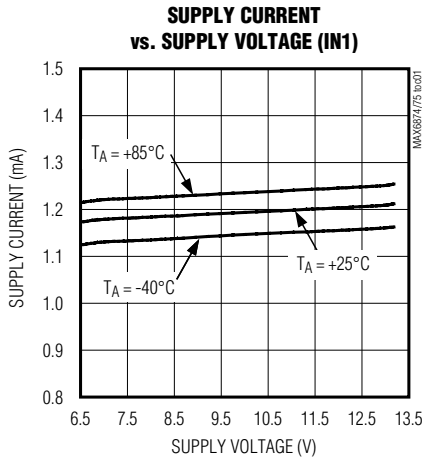
Note 5: Input filters on SDA, SCL, A0, and A1 suppress noise spikes $< 50ns$.

Note 6: An additional cycle is required when writing to configuration memory for the first time.

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Typical Operating Characteristics

($V_{IN1} = +6.5V$ to $+13.2V$, $V_{IN2-VIN6} = +2.7V$ to $+5.5V$, $GPI_{-} = GND$, $MARGIN = MR = DBP$, $T_A = +25^{\circ}C$, unless otherwise noted.)

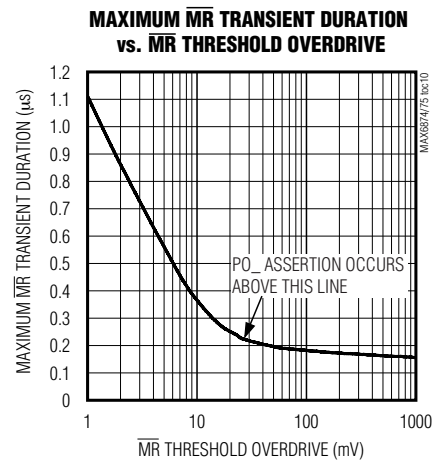
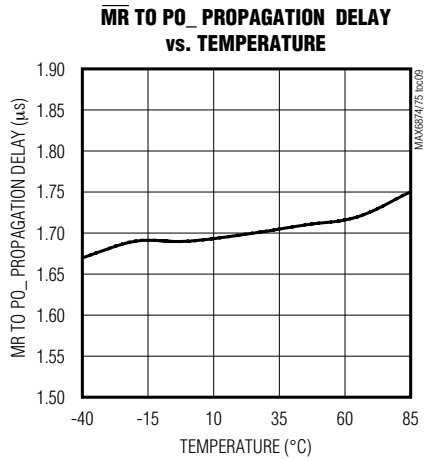
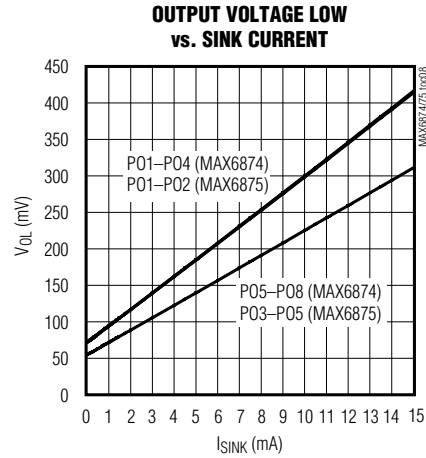
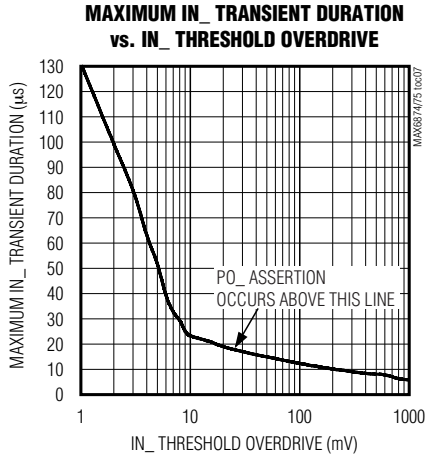


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MAX6874/MAX6875

Typical Operating Characteristics (continued)

(V_{IN1} = +6.5V to +13.2V, V_{IN2} - V_{IN6} = +2.7V to +5.5V, GPI_{-} = GND, \overline{MARGIN} = \overline{MR} = DBP, T_A = +25°C, unless otherwise noted.)



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Pin Description

| PIN | | NAME | FUNCTION |
|---------------|--------------------------------|----------------------------|--|
| MAX6874 | MAX6875 | | |
| 1 | 3 | PO2 | Programmable Output 2. Configurable active-high or active-low open-drain output. PO2 pulls low with a 10 μ A internal current sink for +1V < V _{ABP} < V _{UVLO} . PO2 assumes its programmed conditional output state when ABP exceeds UVLO. |
| 2 | 5 | PO3 | Programmable Output 3. Configurable active-high or active-low open-drain output. PO3 pulls low with a 10 μ A internal current sink for +1V < V _{ABP} < V _{UVLO} . PO3 assumes its programmed conditional output state when ABP exceeds UVLO. |
| 3 | 6 | PO4 | Programmable Output 4. Configurable active-high or active-low open-drain output. PO4 pulls low with a 10 μ A internal current sink for +1V < V _{ABP} < V _{UVLO} . PO4 assumes its programmed conditional output state when ABP exceeds UVLO. |
| 4 | 4 | GND | Ground |
| 5 | 7 | PO5 | Programmable Output 5. Configurable active-high or active-low open-drain output. PO5 pulls low with a 10 μ A internal current sink for +1V < V _{ABP} < V _{UVLO} . PO5 assumes its programmed conditional output state when ABP exceeds UVLO. |
| 6 | — | PO6 | Programmable Output 6. Configurable active-high or active-low open-drain output. PO6 pulls low with a 10 μ A internal current sink for +1V < V _{ABP} < V _{UVLO} . PO6 assumes its programmed conditional output state when ABP exceeds UVLO. |
| 7 | — | PO7 | Programmable Output 7. Configurable active-high or active-low open-drain output. PO7 pulls low with a 10 μ A internal current sink for +1V < V _{ABP} < V _{UVLO} . PO7 assumes its programmed conditional output state when ABP exceeds UVLO. |
| 8 | — | PO8 | Programmable Output 8. Configurable active-high or active-low open-drain output. PO8 pulls low with a 10 μ A internal current sink for +1V < V _{ABP} < V _{UVLO} . PO8 assumes its programmed conditional output state when ABP exceeds UVLO. |
| 9, 10, 23, 24 | 1, 8, 9, 10, 16, 17, 23–26, 32 | N.C. | No Connection. Not internally connected. |
| 11 | 11 | $\overline{\text{MARGIN}}$ | Margin Input. Drive $\overline{\text{MARGIN}}$ low to hold PO _n in their existing states. Leave $\overline{\text{MARGIN}}$ unconnected or connect to DBP if unused. $\overline{\text{MARGIN}}$ overrides $\overline{\text{MR}}$ if both assert at the same time. $\overline{\text{MARGIN}}$ is internally pulled up to DBP through a 10 μ A current source. |
| 12 | 12 | $\overline{\text{MR}}$ | Manual Reset Input. $\overline{\text{MR}}$ to either assert PO _n into a programmed state or to have no effect on PO _n when driving $\overline{\text{MR}}$ low (see Table 6). Leave $\overline{\text{MR}}$ unconnected or connect to DBP if unused. $\overline{\text{MR}}$ is internally pulled up to DBP through a 10 μ A current source. |
| 13 | 13 | SDA | Serial Data Input/Output (Open-Drain). SDA requires an external pullup resistor. |
| 14 | 14 | SCL | Serial Clock Input. SCL requires an external pullup resistor. |
| 15 | 15 | A0 | Address Input 0. Address inputs allow up to four MAX6874 or two MAX6875 connections on one common bus. Connect A0 to GND or to the serial interface power supply. |
| 16 | — | A1 | Address Input 1 (MAX6874 only). Address inputs allow up to four MAX6874 connections on one common bus. Connect A1 to GND or to the serial interface power supply. |

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Pin Description (continued)

MAX6874/MAX6875

| PIN | | NAME | FUNCTION |
|---------|---------|------|---|
| MAX6874 | MAX6875 | | |
| 17 | — | GPI4 | General-Purpose Logic Input 4 (MAX6874 Only). An internal 10 μ A current source pulls GPI4 to GND. Configure GPI4 to control watchdog timer functions or the programmable outputs. |
| 18 | 18 | GPI3 | General-Purpose Logic Input 3. An internal 10 μ A current source pulls GPI3 to GND. Configure GPI3 to control watchdog timer functions or the programmable outputs. |
| 19 | 19 | GPI2 | General-Purpose Logic Input 2. An internal 10 μ A current source pulls GPI2 to GND. Configure GPI2 to control watchdog timer functions or the programmable outputs. |
| 20 | 20 | GPI1 | General-Purpose Logic Input 1. An internal 10 μ A current source pulls GPI1 to GND. Configure GPI1 to control watchdog timer functions or the programmable outputs. |
| 21 | 21 | ABP | Internal Power-Supply Output. Bypass ABP to GND with a 1 μ F ceramic capacitor. ABP powers the internal circuitry of the MAX6874/MAX6875. Do not use ABP to supply power to external circuitry. |
| 22 | 22 | DBP | Internal Digital Power-Supply Output. Bypass DBP to GND with a 1 μ F ceramic capacitor. DBP supplies power to the EEPROM memory and the internal logic circuitry. Do not use DBP to supply power to external circuitry. |
| 25 | — | IN6 | Voltage Input 6. Configure IN6 to detect voltage thresholds between +1V and +5.5V in 20mV increments, or +0.5V to +3.05V in 10mV increments. For improved noise immunity, bypass IN6 to GND with a 0.1 μ F capacitor installed as close to the device as possible. |
| 26 | — | IN5 | Voltage Input 5. Configure IN5 to detect voltage thresholds between +1V and +5.5V in 20mV increments, or +0.5V to +3.05V in 10mV increments. For improved noise immunity, bypass IN5 to GND with a 0.1 μ F capacitor installed as close to the device as possible. |
| 27 | 27 | IN4 | Voltage Input 4. Configure IN4 to detect voltage thresholds between +1V and +5.5V in 20mV increments, or +0.5V to +3.05V in 10mV increments. For improved noise immunity, bypass IN4 to GND with a 0.1 μ F capacitor installed as close to the device as possible. |
| 28 | 28 | IN3 | Voltage Input 3. Configure IN3 to detect voltage thresholds between +1V and +5.5V in 20mV increments, or +0.5V to +3.05V in 10mV increments. For improved noise immunity, bypass IN3 to GND with a 0.1 μ F capacitor installed as close to the device as possible. |
| 29 | 29 | IN2 | Voltage Input 2. Configure IN2 to detect voltage thresholds from +2.5V to +5.5V in 50mV increments or +1.25V to +3.05V in 25mV increments. For improved noise immunity, bypass IN2 to GND with a 0.1 μ F capacitor installed as close to the device as possible. |
| 30 | 30 | IN1 | High-Voltage Input 1. Configure IN1 to detect voltage thresholds from +2.5V to +13.2V in 50mV increments or +1.25V to +7.6V in 25mV increments. For improved noise immunity, bypass IN1 to GND with a 0.1 μ F capacitor installed as close to the device as possible. |
| 31 | 31 | I.C. | Internal Connection. Leave unconnected. |
| 32 | 2 | PO1 | Programmable Output 1. Configurable active-high or active-low open-drain output. PO1 pulls low with a 10 μ A internal current sink for +1V < V _{ABP} < V _{UVLO} . PO1 assumes its programmed conditional output state when ABP exceeds UVLO. |
| — | — | EP | Exposed Paddle. Exposed paddle is internally connected to GND. |

EEPROM-Programmable, Hex/Quad, Power-Supply Sequencers/Supervisors

Detailed Description

The MAX6874/MAX6875 EEPROM-configurable, multi-voltage supply sequencers/supervisors monitor several voltage detector inputs and general-purpose logic inputs, and feature programmable outputs for highly configurable power-supply sequencing applications. The MAX6874 features six voltage detector inputs, four general-purpose logic inputs, and eight programmable outputs, while the MAX6875 features four voltage detector inputs, three general-purpose logic inputs, and five programmable outputs. Manual reset and margin disable inputs simplify board-level testing during the manufacturing process. The MAX6874/MAX6875 feature an accurate internal 1.25V reference.

All voltage detectors provide configurable thresholds for undervoltage detection. One high-voltage input (IN1) provides detector threshold voltages from +1.25V to +7.625V in 25mV increments or +2.5V to +13.2V in 50mV increments. A positive input (IN2) provides detector threshold voltages from +1.25V to +3.05V in 25mV increments or +2.5V to +5.5V in 50mV increments. Positive inputs (IN3–IN6) provide detector threshold voltages from +0.5V to +3.05V in 10mV increments or +1.0V to +5.5V in 20mV increments.

The host controller communicates with the MAX6874/MAX6875's internal 4kb user EEPROM, configuration

EEPROM, and configuration registers through an SMBus/I²C-compatible serial interface (see Figure 1).

Program the open-drain outputs as active-high or active-low. Program each output to assert on any voltage detector input, general-purpose logic input, watchdog timer, manual reset, or other output stages. Programmable timing delay blocks configure each output to wait between 25µs and 1600ms before de-asserting.

The MAX6874/MAX6875 feature a watchdog timer, adding flexibility. Program the watchdog timer to assert one or more programmable outputs. Program the watchdog timer to clear on a combination of one GPI_ input and one programmable output, one of the GPI_ inputs only, or one of the programmable outputs only. The initial and normal watchdog timeout periods are independently programmable from 6.25ms to 102.4s.

A virtual diode-ORing scheme selects the input that powers the MAX6874/MAX6875. The MAX6874/MAX6875 derive power from IN1 if $V_{IN1} > +6.5V$ or from the highest voltage on IN3–IN5 if $V_{IN1} < +2.7V$. The power source cannot be determined if $+4V < V_{IN1} < +6.5V$ and one of V_{IN3} through $V_{IN5} > +2.7V$. The programmable outputs maintain the correct programmed logic state for $V_{ABP} > V_{UVLO}$. One of IN3 through IN5 must be greater than +2.7V or IN1 must be greater than +4V for device operation.

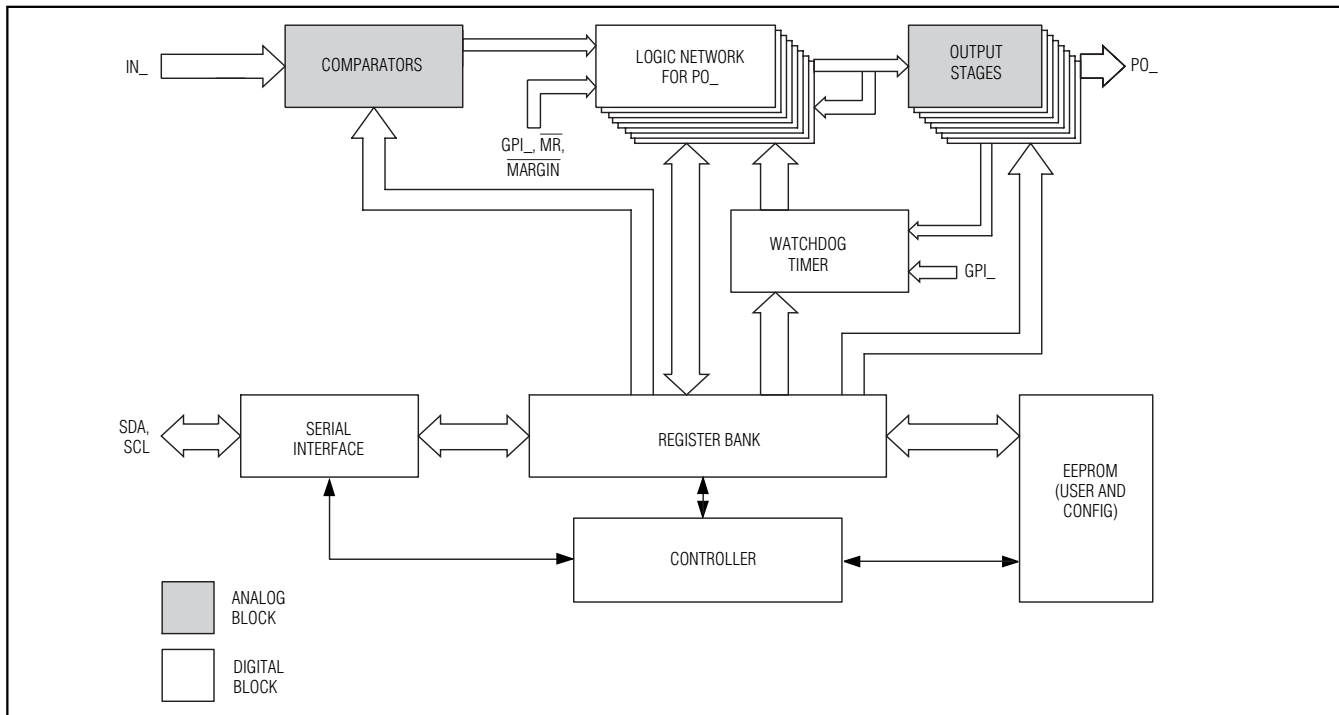
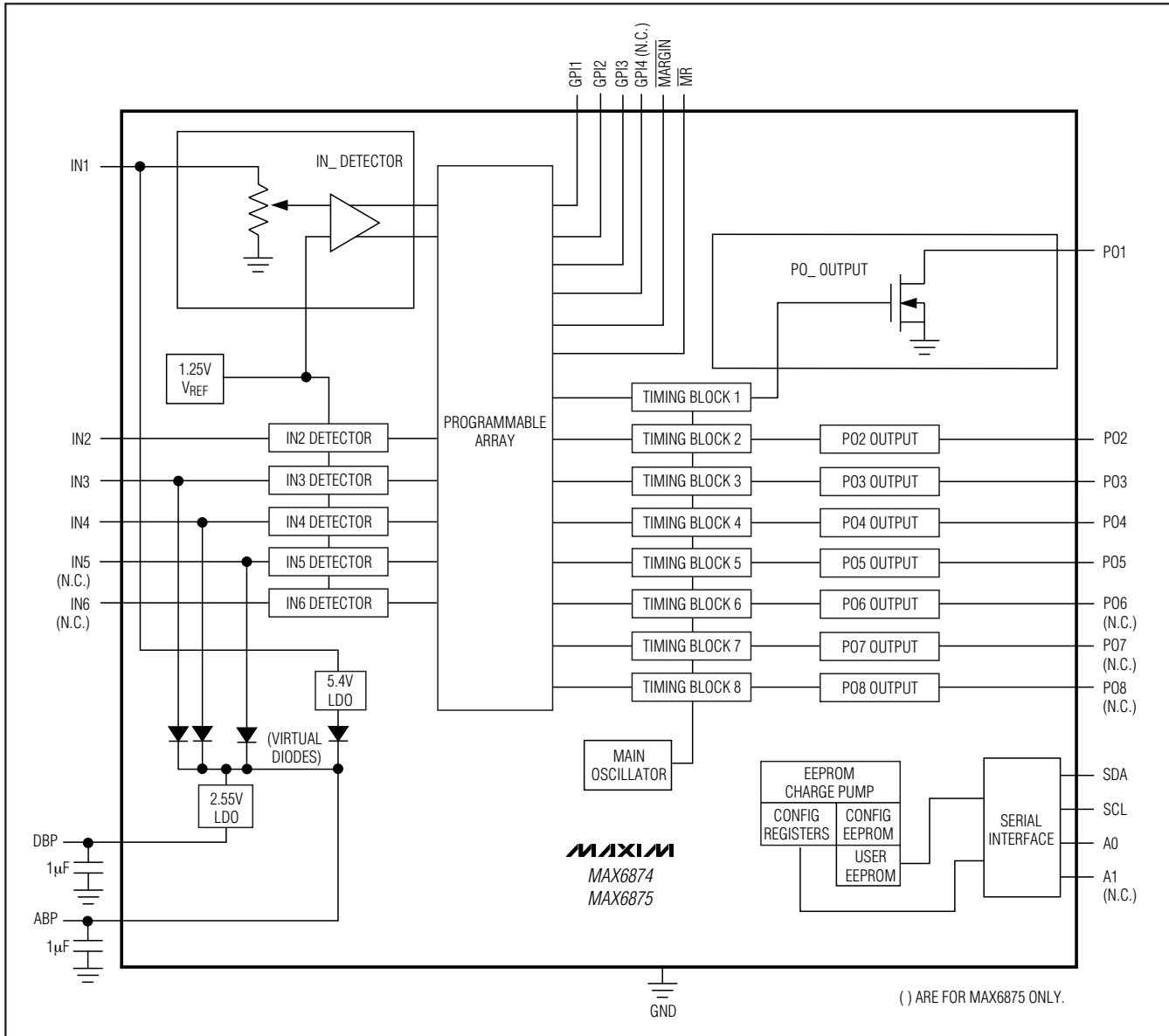


Figure 1. Top-Level Block Diagram

EEPROM-Programmable, Hex/Quad, Power-Supply Sequencers/Supervisors

Functional Diagram

MAX6874/MAX6875



EEPROM-Programmable, Hex/Quad, Power-Supply Sequencers/Supervisors

Powering the MAX6874/MAX6875

The MAX6874/MAX6875 derive power from the positive voltage-detector inputs: IN1 or IN3–IN5. A virtual diode-ORing scheme selects the positive input that supplies power to the device (see the *Functional Diagram*). IN1 must be at least +4V or one of IN3–IN5 (MAX6874)/IN3–IN4 (MAX6875) must be at least +2.7V to ensure device operation. An internal LDO regulates IN1 down to +5.4V.

The highest input voltage on IN3–IN5 (MAX6874)/IN3–IN4 (MAX6875) supplies power to the device, unless $V_{IN1} \geq +6.5V$, in which case IN1 supplies power to the device. For $+4V < V_{IN1} < +6.5V$ and one of V_{IN3} through $V_{IN5} > +2.7V$, the input power source cannot be determined due to the dropout voltage of the LDO. Internal hysteresis ensures that the supply input that initially powered the device continues to power the device when multiple input voltages are within 50mV of each other.

ABP powers the analog circuitry; bypass ABP to GND with a 1 μ F ceramic capacitor installed as close to the

device as possible. The internal supply voltage, measured at ABP, equals the maximum of IN3–IN5 (MAX6874)/IN3–IN4 (MAX6875) if $V_{IN1} = 0$, or equals +5.4V when $V_{IN1} > +6.5V$. Do not use ABP to provide power to external circuitry.

The MAX6874/MAX6875 also generate a digital supply voltage (DBP) for the internal logic circuitry and the EEPROM; bypass DBP to GND with a 1 μ F ceramic capacitor installed as close to the device as possible. The nominal DBP output voltage is +2.55V. Do not use DBP to provide power to external circuitry.

Inputs

The MAX6874/MAX6875 contain multiple logic and voltage-detector inputs. Table 1 summarizes these various inputs.

Set the threshold voltages for each voltage-detector input with registers 00h–05h. Each threshold voltage is an undervoltage threshold. Set the threshold range for each voltage detector with register 0Dh.

Table 1. Programmable Features

| FEATURE | DESCRIPTION |
|--|--|
| High-Voltage Input (IN1) | <ul style="list-style-type: none"> Undervoltage threshold +2.5V to +13.2V threshold in 50mV increments +1.25V to +7.625V threshold in 25mV increments |
| Voltage Input (IN2) | <ul style="list-style-type: none"> Undervoltage threshold +2.5V to +5.5V threshold in 50mV increments +1.25V to +3.05V threshold in 25mV increments |
| Voltage Input IN3–IN6 (MAX6874), IN3–IN4 (MAX6875) | <ul style="list-style-type: none"> Undervoltage threshold +1V to +5.5V threshold in 20mV increments +0.5V to +3.05V threshold in 10mV increments |
| Programmable Outputs PO1–PO8 (MAX6874), PO1–PO5 (MAX6875) | <ul style="list-style-type: none"> Active high or active low Open-drain output Dependent on \overline{MR}, \overline{MARGIN}, $IN_{_}$, GPI1–GPI4, WD, and/or $PO_{_}$ Programmable timeout periods of 25μs, 1.5625ms, 6.25ms, 25ms, 50ms, 200ms, 400ms, or 1.6s |
| General-Purpose Logic Inputs, GPI1–GPI4 (MAX6874), GPI1–GPI3 (MAX6875) | <ul style="list-style-type: none"> Active-high or active-low logic levels Configure GPI$_{_}$ as inputs to watchdog timers or programmable output stages |
| Watchdog Timer | <ul style="list-style-type: none"> Clear dependent on any combination of one GPI$_{_}$ input and one programmable output, a GPI$_{_}$ input only, or a programmable output only Initial watchdog timeout period of 6.25ms, 25ms, 100ms, 400ms, 1.6s, 6.4s, 25.6s, or 102.4s Normal watchdog timeout period of 6.25ms, 25ms, 100ms, 400ms, 1.6s, 6.4s, 25.6s, or 102.4s Watchdog enable/disable |

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Table 1. Programmable Features (continued)

| FEATURE | DESCRIPTION |
|-------------------------|---|
| Manual Reset Input (MR) | <ul style="list-style-type: none"> • Forces PO_ into the active output state when $\overline{MR} = \text{GND}$ • PO_ deassert after MR releases high and the PO_ timeout period expires • PO_ cannot be a function of MR only |
| Write Disable | <ul style="list-style-type: none"> • Locks user EEPROM based on PO_ |
| Configuration Lock | <ul style="list-style-type: none"> • Locks configuration EEPROM |

High-Voltage Input (IN1)

IN1 offers threshold voltages of +2.5V to +13.2V in 50mV increments, or +1.25V to +7.625V in 25mV increments. Use the following equations to set the threshold voltages for IN1:

$$x = \frac{V_{TH} - 2.5V}{0.05V} \text{ for } +2.5V \text{ to } +13.2V \text{ range}$$

$$x = \frac{V_{TH} - 1.25V}{0.025V} \text{ for } +1.25V \text{ to } +7.625V \text{ range}$$

where V_{TH} is the desired threshold voltage and x is the decimal code for the desired threshold (Table 2). For the +2.5V to +13.2V range, x must equal 214 or less, otherwise the threshold exceeds the maximum operating voltage of IN1.

IN2

IN2 offers thresholds from +2.5V to +5.5V in 50mV increments, or +1.25V to +3.05V in 25mV increments. Use the following equations to set the threshold voltages for IN2:

$$x = \frac{V_{TH} - 2.5V}{0.05V} \text{ for } +2.5V \text{ to } +5.5V \text{ range}$$

$$x = \frac{V_{TH} - 1.25V}{0.025V} \text{ for } +1.25V \text{ to } +3.05V \text{ range}$$

where V_{TH} is the desired threshold voltage and x is the decimal code for the desired threshold (Table 3).

For the +2.5V to +5.5V range, x must equal 60 or less, otherwise the threshold exceeds the maximum operating voltage of IN2. For the +1V to +3.05V range, x must equal 72 or less.

IN3–IN6

IN3–IN6 offer positive voltage detectors monitor voltages from +1V to +5.5V in 20mV increments, or +0.5V to +3.05V in 10mV increments. Use the following equations to set the threshold voltages for IN_:

$$x = \frac{V_{TH} - 1V}{0.02V} \text{ for } +1V \text{ to } +5.5V \text{ range}$$

$$x = \frac{V_{TH} - 0.5V}{0.01V} \text{ for } +0.5V \text{ to } +3.05V \text{ range}$$

where V_{TH} is the desired threshold voltage and x is the decimal code for the desired threshold (Table 4). For the +1V to +5.5V range, x must equal 225 or less, otherwise the threshold exceeds the maximum operating voltage of IN3–IN6.

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Table 2. IN1 Threshold Settings

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | DESCRIPTION |
|------------------|-----------------------|-----------|---|
| 00h | 8000h | [7:0] | IN1 detector threshold (V1) (see equations in the <i>High-Voltage Input (IN1)</i> section). |
| 0Dh | 800Dh | [0] | IN1 range selection: 0 = 2.5V to 13.2V range in 50mV increments. 1 = 1.25V to 7.625V range in 25mV increments. |

Table 3. IN2 Threshold Settings

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | DESCRIPTION |
|------------------|-----------------------|-----------|--|
| 01h | 8001h | [7:0] | IN2 detector threshold (V2) (see equations in the <i>IN2</i> section). |
| 0Dh | 800Dh | [7:6] | IN2 range selection: 00 = Not used. 01 = Not used. 10 = +2.5V to +5.5V range in 50mV increments. 11 = +1.25V to +3.05V range in 25mV increments. |

Table 4. IN3–IN6 Threshold Settings

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | DESCRIPTION |
|------------------|-----------------------|-----------|---|
| 02h | 8002h | [7:0] | IN3 detector threshold (V3) (see equations in the <i>IN3–IN6</i> section). |
| 03h | 8003h | [7:0] | IN4 detector threshold (V4) (see equations in the <i>IN3–IN6</i> section). |
| 04h | 8004h | [7:0] | IN5 (MAX6874 only) detector threshold (V5) (see equations in the <i>IN3–IN6</i> section). |
| 05h | 8005h | [7:0] | IN6 (MAX6874 only) detector threshold (V6) (see equations in the <i>IN3–IN6</i> section). |
| 0Dh | 800Dh | [1] | IN3 range selection: 0 = +1V to +5.5V range in 20mV increments. 1 = +0.5V to +3.05V range in 10mV increments. |
| | | [2] | IN4 range selection: 0 = +1V to +5.5V range in 20mV increments. 1 = +0.5V to +3.05V range in 10mV increments. |
| | | [3] | IN5 (MAX6874 only) range selection: 0 = +1V to +5.5V range in 20mV increments. 1 = +0.5V to +3.05V range in 10mV increments. |
| | | [4] | IN6 (MAX6874 only) range selection: 0 = +1V to +5.5V range in 20mV increments. 1 = +0.5V to +3.05V range in 10mV increments. |
| | | [5] | Not used. |

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MAX6874/MAX6875

GPI1–GPI4 (MAX6874)/GPI1–GPI3 (MAX6875)

The GPI1–GPI4 programmable logic inputs control power-supply sequencing (programmable outputs), reset/interrupt signaling, and watchdog functions (see the *Configuring the Watchdog Timer (Registers 3Ch–3Dh)* section). Configure GPI1–GPI4 for active-low or active-high logic (Table 5). GPI1–GPI4 internally pull down to GND through a 10µA current sink.

\overline{MR}

The manual reset (\overline{MR}) input initiates a reset condition. Register 40h determines the programmable outputs that assert while \overline{MR} is low (Table 6). All affected programmable outputs remain asserted (see the *Programmable Outputs* section) for their PO_ timeout periods after \overline{MR} releases high. An internal 10µA current source pulls \overline{MR} to DBP. Leave \overline{MR} unconnected or connect to DBP if unused. A programmable output cannot depend solely on \overline{MR} .

\overline{MARGIN}

\overline{MARGIN} allows system-level testing while power supplies exceed the normal ranges. Drive \overline{MARGIN} low to hold the programmable outputs in their state while system-level testing occurs. Leave \overline{MARGIN} unconnected or connect to DBP if unused. An internal 10µA current source pulls \overline{MARGIN} to DBP. The state of each programmable output does not change while $\overline{MARGIN} = \text{GND}$. \overline{MARGIN} overrides \overline{MR} if both assert at the same time.

Programmable Outputs

The MAX6874 features eight programmable outputs while the MAX6875 features five programmable outputs. Program the open-drain outputs as active-high or active-low. During power-up, the programmable outputs pull to GND with an internal 10µA current sink for $1V < V_{ABP} < V_{UVLO}$. The programmable outputs remain in their active states until their respective timeout periods (PO_) expire and all of the programmed conditions are met for each output. Any output programmed to depend

Table 5. GPI1–GPI4 Active Logic States

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | DESCRIPTION |
|------------------|-----------------------|-----------|---|
| 3Bh | 803Bh | [0] | GPI1. 0 = active low. 1 = active high. |
| | | [1] | GPI2. 0 = active low. 1 = active high. |
| | | [2] | GPI3. 0 = active low. 1 = active high. |
| | | [3] | GPI4 (MAX6874 only). 0 = active low. 1 = active high. |

Table 6. Programmable Output Behavior and \overline{MR}

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | DESCRIPTION |
|------------------|-----------------------|-----------|---|
| 40h | 8040h | [0] | PO1 (MAX6874 only). 0 = PO1 independent of \overline{MR} . 1 = PO1 asserts when $\overline{MR} = \text{low}$. |
| | | [1] | PO2 (MAX6874 only). 0 = PO2 independent of \overline{MR} . 1 = PO2 asserts when $\overline{MR} = \text{low}$. |
| | | [2] | PO3 (MAX6874)/PO1 (MAX6875). 0 = PO3/PO1 independent of \overline{MR} . 1 = PO3/PO1 asserts when $\overline{MR} = \text{low}$. |
| | | [3] | PO4 (MAX6874)/PO2 (MAX6875). 0 = PO4/PO2 independent of \overline{MR} . 1 = PO4/PO2 asserts when $\overline{MR} = \text{low}$. |
| | | [4] | PO5 (MAX6874)/PO3 (MAX6875). 0 = PO5/PO3 independent of \overline{MR} . 1 = PO5/PO3 asserts when $\overline{MR} = \text{low}$. |
| | | [5] | PO6 (MAX6874)/PO4 (MAX6875). 0 = PO6/PO4 independent of \overline{MR} . 1 = PO6/PO4 asserts when $\overline{MR} = \text{low}$. |
| | | [6] | PO7 (MAX6874)/PO5 (MAX6875). 0 = PO7/PO5 independent of \overline{MR} . 1 = PO7/PO5 asserts when $\overline{MR} = \text{low}$. |
| | | [7] | PO8 (MAX6874 only). 0 = PO8 independent of \overline{MR} . 1 = PO8 asserts when $\overline{MR} = \text{low}$. |

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Table 7. PO1 (MAX6874 Only) Output Dependency

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT | OUTPUT ASSERTION CONDITIONS |
|------------------|-----------------------|-------|--|
| 0Eh | 800Eh | [0] | 1 = PO1 assertion depends on IN1 undervoltage threshold (Table 2). |
| | | [1] | 1 = PO1 assertion depends on IN2 undervoltage threshold (Table 3). |
| | | [2] | 1 = PO1 assertion depends on IN3 undervoltage threshold (Table 4). |
| | | [3] | 1 = PO1 assertion depends on IN4 undervoltage threshold (Table 4). |
| | | [4] | 1 = PO1 assertion depends on IN5 undervoltage threshold (Table 4). |
| | | [5] | 1 = PO1 assertion depends on IN6 undervoltage threshold (Table 4). |
| | | [6] | 1 = PO1 assertion depends on watchdog (Tables 19 and 20). |
| | | [7] | Must be set to 0. |
| 0Fh | 800Fh | [5:0] | Must be set to 0. |
| | | [6] | 1 = PO1 assertion depends on GPI1 (Table 5). |
| | | [7] | 1 = PO1 assertion depends on GPI2 (Table 5). |
| 10h | 8010h | [0] | 1 = PO1 assertion depends on GPI3 (Table 5). |
| | | [1] | 1 = PO1 assertion depends on GPI4 (Table 5). |
| | | [2] | 1 = PO1 assertion depends on PO2 (Table 8). |
| | | [3] | 1 = PO1 assertion depends on PO3 (Table 9). |
| | | [4] | 1 = PO1 assertion depends on PO4 (Table 10). |
| | | [5] | 1 = PO1 assertion depends on PO5 (Table 11). |
| | | [6] | 1 = PO1 assertion depends on PO6 (Table 12). |
| | | [7] | 1 = PO1 assertion depends on PO7 (Table 13). |
| 11h | 8011h | [0] | 1 = PO1 assertion depends on PO8 (Table 14). |
| 40h | 8040h | [0] | 1 = PO1 asserts when \overline{MR} = low (Table 6). |

on no condition always remains in its active state (Table 19). An output configured as active-high is considered asserted when that output is logic high. No output can depend solely on \overline{MR} .

The voltage monitors generate fault signals (logical 0) to the MAX6874/MAX6875s' logic array when an input voltage is below the programmed undervoltage threshold.

Registers 0Eh through 3Ah and 40h configure each of the programmable outputs. Programmable timing blocks set the PO_ timeout period from 25 μ s to 1600ms for each programmable output. See register 3Ah (Table 15) to set the active state (active-high or active-low) for each programmable output and Table 16 for timeout periods for each output.

For example, PO3 (MAX6874—Table 9) may depend on the IN1 undervoltage threshold, and the states of GPI1, PO1, and PO2. Write a one to R16h[0], R17h[6], and R18h[3:2] to configure the output as indicated. IN1 must be above the undervoltage threshold (Table 2), GPI1 must be inactive (Table 5), and PO1 (Tables 7 and 15) and PO2 (Table 9) must be in their deasserted states for the output to deassert.

Table 7 only applies to PO1 of the MAX6874. Write a 0 to a bit to make the PO1 output independent of the respective signal (IN1–IN6 thresholds, WD, GPI1–GPI4, \overline{MR} , or other programmable outputs).

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Table 8. PO2 (MAX6874 Only) Output Dependency

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT | OUTPUT ASSERTION CONDITIONS |
|------------------|-----------------------|-------|--|
| 12h | 8012h | [0] | 1 = PO2 assertion depends on IN1 undervoltage threshold (Table 2). |
| | | [1] | 1 = PO2 assertion depends on IN2 undervoltage threshold (Table 3). |
| | | [2] | 1 = PO2 assertion depends on IN3 undervoltage threshold (Table 4). |
| | | [3] | 1 = PO2 assertion depends on IN4 undervoltage threshold (Table 4). |
| | | [4] | 1 = PO2 assertion depends on IN5 undervoltage threshold (Table 4). |
| | | [5] | 1 = PO2 assertion depends on IN6 undervoltage threshold (Table 4). |
| | | [6] | 1 = PO2 assertion depends on watchdog (Tables 18 and 19). |
| | | [7] | Must be set to 0. |
| 13h | 8013h | [5:0] | Must be set to 0. |
| | | [6] | 1 = PO2 assertion depends on GPI1 (Table 5). |
| | | [7] | 1 = PO2 assertion depends on GPI2 (Table 5). |
| 14h | 8014h | [0] | 1 = PO2 assertion depends on GPI3 (Table 5). |
| | | [1] | 1 = PO2 assertion depends on GPI4 (Table 5). |
| | | [2] | 1 = PO2 assertion depends on PO1 (Table 7). |
| | | [3] | 1 = PO2 assertion depends on PO3 (Table 9). |
| | | [4] | 1 = PO2 assertion depends on PO4 (Table 10). |
| | | [5] | 1 = PO2 assertion depends on PO5 (Table 11). |
| | | [6] | 1 = PO2 assertion depends on PO6 (Table 12). |
| | | [7] | 1 = PO2 assertion depends on PO7 (Table 13). |
| 15h | 8015h | [0] | 1 = PO2 assertion depends on PO8 (Table 14). |
| 40h | 8040h | [1] | 1 = PO2 asserts when \overline{MR} = low (Table 6). |

Table 8 only applies to PO2 of the MAX6874. Write a 0 to a bit to make the PO2 output independent of the

respective signal (IN1–IN6 thresholds, WD, GPI1–GPI4, \overline{MR} , or other programmable outputs).

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Table 9. PO3 (MAX6874)/PO1 (MAX6875) Output Dependency

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT | OUTPUT ASSERTION CONDITIONS |
|------------------|-----------------------|-------|---|
| 16h | 8016h | [0] | 1 = PO3/PO1 assertion depends on IN1 undervoltage threshold (Table 2). |
| | | [1] | 1 = PO3/PO1 assertion depends on IN2 undervoltage threshold (Table 3). |
| | | [2] | 1 = PO3/PO1 assertion depends on IN3 undervoltage threshold (Table 4). |
| | | [3] | 1 = PO3/PO1 assertion depends on IN4 undervoltage threshold (Table 4). |
| | | [4] | 1 = PO3 (MAX6874 only) assertion depends on IN5 undervoltage threshold (Table 4). Must be set to 0 for the MAX6875. |
| | | [5] | 1 = PO3 (MAX6874 only) assertion depends on IN6 undervoltage threshold (Table 4). Must be set to 0 for the MAX6875. |
| | | [6] | 1 = PO3/PO1 assertion depends on watchdog (Tables 18 and 19). |
| | | [7] | Must be set to 0. |
| 17h | 8017h | [5:0] | Must be set to 0. |
| | | [6] | 1 = PO3/PO1 assertion depends on GPI1 (Table 5). |
| | | [7] | 1 = PO3/PO1 assertion depends on GPI2 (Table 5). |
| 18h | 8018h | [0] | 1 = PO3/PO1 assertion depends on GPI3 (Table 5). |
| | | [1] | 1 = PO3/PO1 assertion depends on GPI4 (Table 5). |
| | | [2] | 1 = PO3 (MAX6874 only) assertion depends on PO1 (Table 7). Must be set to 0 for the MAX6875. |
| | | [3] | 1 = PO3 (MAX6874 only) assertion depends on PO2 (Table 8). Must be set to 0 for the MAX6875. |
| | | [4] | 1 = PO3/PO1 assertion depends on PO4 (MAX6874)/PO2 (MAX6875) (Table 10). |
| | | [5] | 1 = PO3/PO1 assertion depends on PO5 (MAX6874)/PO3 (MAX6875) (Table 11). |
| | | [6] | 1 = PO3/PO1 assertion depends on PO6 (MAX6874)/PO4 (MAX6875) (Table 12). |
| | | [7] | 1 = PO3/PO1 assertion depends on PO7 (MAX6874)/PO5 (MAX6875) (Table 13). |
| 1Ch | 801Ch | [1:0] | 1 = PO3 (MAX6874 only) assertion depends on PO8 (Table 14). Must be set to 0 for the MAX6875. |
| 40h | 8040h | [2] | 1 = PO3/PO1 asserts when \overline{MR} = low (Table 6). |

Table 9 only applies to PO3 of the MAX6874 and PO1 of the MAX6875. Write a 0 to a bit to make the PO3/PO1 output independent of the respective signal (IN_

thresholds, WD, GPI1–GPI4, \overline{MR} , or other programmable outputs).

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Table 10. PO4 (MAX6874)/PO2 (MAX6875) Output Dependency

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT | OUTPUT ASSERTION CONDITIONS |
|------------------|-----------------------|-------|---|
| 1Dh | 801Dh | [0] | 1 = PO4/PO2 assertion depends on IN1 undervoltage threshold (Table 2). |
| | | [1] | 1 = PO4/PO2 assertion depends on IN2 undervoltage threshold (Table 3). |
| | | [2] | 1 = PO4/PO2 assertion depends on IN3 undervoltage threshold (Table 4). |
| | | [3] | 1 = PO4/PO2 assertion depends on IN4 undervoltage threshold (Table 4). |
| | | [4] | 1 = PO4 (MAX6874 only) assertion depends on IN5 undervoltage threshold (Table 4). Must be set to 0 for the MAX6875. |
| | | [5] | 1 = PO4 (MAX6874 only) assertion depends on IN6 undervoltage threshold (Table 4). Must be set to 0 for the MAX6875. |
| | | [6] | 1 = PO4/PO2 assertion depends on watchdog (Tables 18 and 19). |
| | | [7] | Must be set to 0. |
| 1Eh | 801Eh | [5:0] | Must be set to 0. |
| | | [6] | 1 = PO4/PO2 assertion depends on GPI1 (Table 5). |
| | | [7] | 1 = PO4/PO2 assertion depends on GPI2 (Table 5). |
| 1Fh | 801Fh | [0] | 1 = PO4/PO2 assertion depends on GPI3 (Table 5). |
| | | [1] | 1 = PO4/PO2 assertion depends on GPI4 (Table 5). |
| | | [2] | 1 = PO4 (MAX6874 only) assertion depends on PO1 (Table 7). Must be set to 0 for the MAX6875. |
| | | [3] | 1 = PO4 (MAX6874 only) assertion depends on PO2 (Table 8). Must be set to 0 for the MAX6875. |
| | | [4] | 1 = PO4/PO2 assertion depends on PO3 (MAX6874)/PO1 (MAX6875) (Table 9). |
| | | [5] | 1 = PO4/PO2 assertion depends on PO5 (MAX6874)/PO3 (MAX6875) (Table 11). |
| | | [6] | 1 = PO4/PO2 assertion depends on PO6 (MAX6874)/PO4 (MAX6875) (Table 12). |
| | | [7] | 1 = PO4/PO2 assertion depends on PO7 (MAX6874)/PO5 (MAX6875) (Table 13). |
| 23h | 8023h | [0] | 1 = PO4 (MAX6874 only) assertion depends on PO8 (Table 14). Must be set to 0 for the MAX6875. |
| 40h | 8040h | [3] | 1 = PO4/PO2 asserts when \overline{MR} = low (Table 6). |

Table 10 only applies to PO4 of the MAX6874 and PO2 of the MAX6875. Write a 0 to a bit to make the PO4/PO2 output independent of the respective signal (IN_

thresholds, WD, GPI1–GPI4, \overline{MR} , or other programmable outputs).

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Table 11. PO5 (MAX6874)/PO3 (MAX6875) Output Dependency

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT | OUTPUT ASSERTION CONDITIONS |
|------------------|--|-------|---|
| 24h | 8024h | [0] | 1 = PO5/PO3 assertion depends on IN1 undervoltage threshold (Table 2). |
| | | [1] | 1 = PO5/PO3 assertion depends on IN2 undervoltage threshold (Table 3). |
| | | [2] | 1 = PO5/PO3 assertion depends on IN3 undervoltage threshold (Table 4). |
| | | [3] | 1 = PO5/PO3 assertion depends on IN4 undervoltage threshold (Table 4). |
| | | [4] | 1 = PO5 (MAX6874 only) assertion depends on IN5 undervoltage threshold (Table 4). Must be set to 0 for the MAX6875. |
| | | [5] | 1 = PO5 (MAX6874 only) assertion depends on IN6 undervoltage threshold (Table 4). Must be set to 0 for the MAX6875. |
| | | [6] | 1 = PO5/PO3 assertion depends on watchdog (Tables 18 and 19). |
| | | [7] | Must be set to 0. |
| 25h | 8025h | [5:0] | Must be set to 0. |
| | | [6] | 1 = PO5/PO3 assertion depends on GPI1 (Table 5). |
| | | [7] | 1 = PO5/PO3 assertion depends on GPI2 (Table 5). |
| 26h | 8026h | [0] | 1 = PO5/PO3 assertion depends on GPI3 (Table 5). |
| | | [1] | 1 = PO5/PO3 assertion depends on GPI4 (Table 5). |
| | | [2] | 1 = PO5 (MAX6874 only) assertion depends on PO1 (Table 7). Must be set to 0 for the MAX6875. |
| | | [3] | 1 = PO5 (MAX6874 only) assertion depends on PO2 (Table 8). Must be set to 0 for the MAX6875. |
| | | [4] | 1 = PO5/PO3 assertion depends on PO3 (MAX6874)/PO1 (MAX6875) (Table 9). |
| | | [5] | 1 = PO5/PO3 assertion depends on PO4 (MAX6874)/PO2 (MAX6875) (Table 10). |
| | | [6] | 1 = PO5/PO3 assertion depends on PO6 (MAX6874)/PO4 (MAX6875) (Table 12). |
| [7] | 1 = PO5/PO3 assertion depends on PO7 (MAX6874)/PO5 (MAX6875) (Table 13). | | |
| 2Ah | 802Ah | [0] | 1 = PO5 (MAX6874 only) assertion depends on PO8 (Table 14). Must be set to 0 for the MAX6875. |
| 40h | 8040h | [4] | 1 = PO5/PO3 asserts when \overline{MR} = low (Table 6). |

Table 11 only applies to PO5 of the MAX6874 and PO3 of the MAX6875. Write a 0 to a bit to make the PO5/PO3 output independent of the respective signal (IN_

thresholds, WD, GPI1–GPI4, \overline{MR} , or other programmable outputs).

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MAX6874/MAX6875

Table 12. PO6 (MAX6874)/PO4 (MAX6875) Output Dependency

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT | OUTPUT ASSERTION CONDITIONS |
|------------------|-----------------------|-------|---|
| 2Bh | 802Bh | [0] | 1 = PO6/PO4 assertion depends on IN1 undervoltage threshold (Table 2). |
| | | [1] | 1 = PO6/PO4 assertion depends on IN2 undervoltage threshold (Table 3). |
| | | [2] | 1 = PO6/PO4 assertion depends on IN3 undervoltage threshold (Table 4). |
| | | [3] | 1 = PO6/PO4 assertion depends on IN4 undervoltage threshold (Table 4). |
| | | [4] | 1 = PO6 (MAX6874 only) assertion depends on IN5 undervoltage threshold (Table 4). Must be set to 0 for the MAX6875. |
| | | [5] | 1 = PO6 (MAX6874 only) assertion depends on IN6 undervoltage threshold (Table 4). Must be set to 0 for the MAX6875. |
| | | [6] | 1 = PO6/PO4 assertion depends on watchdog (Tables 18 and 19). |
| | | [7] | Must be set to 0. |
| 2Ch | 802Ch | [5:0] | Must be set to 0. |
| | | [6] | 1 = PO6/PO4 assertion depends on GPI1 (Table 5). |
| | | [7] | 1 = PO6/PO4 assertion depends on GPI2 (Table 5). |
| 2Dh | 802Dh | [0] | 1 = PO6/PO4 assertion depends on GPI3 (Table 5). |
| | | [1] | 1 = PO6/PO4 assertion depends on GPI4 (Table 5). |
| | | [2] | 1 = PO6 (MAX6874 only) assertion depends on PO1 (Table 7). Must be set to 0 for the MAX6875. |
| | | [3] | 1 = PO6 (MAX6874 only) assertion depends on PO2 (Table 8). Must be set to 0 for the MAX6875. |
| | | [4] | 1 = PO6/PO4 assertion depends on PO3 (MAX6874)/PO1 (MAX6875) (Table 9). |
| | | [5] | 1 = PO6/PO4 assertion depends on PO4 (MAX6874)/PO2 (MAX6875) (Table 10). |
| | | [6] | 1 = PO6/PO4 assertion depends on PO5 (MAX6874)/PO3 (MAX6875) (Table 11). |
| | | [7] | 1 = PO6/PO4 assertion depends on PO7 (MAX6874)/PO5 (MAX6875) (Table 13). |
| 31h | 8031h | [0] | 1 = PO6 (MAX6874 only) assertion depends on PO8 (Table 14). Must be set to 0 for the MAX6875. |
| 40h | 8040h | [5] | 1 = PO6/PO4 asserts when \overline{MR} = low (Table 6). |

Table 12 only applies to PO6 of the MAX6874 and PO4 of the MAX6875. Write a 0 to a bit to make the PO6/PO4 output independent of the respective signal (IN_

thresholds, WD, GPI1–GPI4, \overline{MR} , or other programmable outputs).

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Table 13. PO7 (MAX6874)/PO5 (MAX6875) Output Dependency

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT | OUTPUT ASSERTION CONDITIONS |
|------------------|-----------------------|-------|---|
| 32h | 8032h | [0] | 1 = PO7/PO5 assertion depends on IN1 undervoltage threshold (Table 2). |
| | | [1] | 1 = PO7/PO5 assertion depends on IN2 undervoltage threshold (Table 3). |
| | | [2] | 1 = PO7/PO5 assertion depends on IN3 undervoltage threshold (Table 4). |
| | | [3] | 1 = PO7/PO5 assertion depends on IN4 undervoltage threshold (Table 4). |
| | | [4] | 1 = PO7 (MAX6874 only) assertion depends on IN5 undervoltage threshold (Table 4). Must be set to 0 for the MAX6875. |
| | | [5] | 1 = PO7 (MAX6874 only) assertion depends on IN6 undervoltage threshold (Table 4). Must be set to 0 for the MAX6875. |
| | | [6] | 1 = PO7/PO5 assertion depends on watchdog (Tables 18 and 19). |
| | | [7] | Must be set to 0. |
| 33h | 8033h | [5:0] | Must be set to 0. |
| | | [6] | 1 = PO7/PO5 assertion depends on GPI1 (Table 5). |
| | | [7] | 1 = PO7/PO5 assertion depends on GPI2 (Table 5). |
| 34h | 8034h | [0] | 1 = PO7/PO5 assertion depends on GPI3 (Table 5). |
| | | [1] | 1 = PO7/PO5 assertion depends on GPI4 (Table 5). |
| | | [2] | 1 = PO7 (MAX6874 only) assertion depends on PO1 (Table 7). Must be set to 0 for the MAX6875. |
| | | [3] | 1 = PO7 (MAX6874 only) assertion depends on PO2 (Table 8). Must be set to 0 for the MAX6875. |
| | | [4] | 1 = PO7/PO5 assertion depends on PO3 (MAX6874)/PO1 (MAX6875) (Table 9). |
| | | [5] | 1 = PO7/PO5 assertion depends on PO4 (MAX6874)/PO2 (MAX6875) (Table 10). |
| | | [6] | 1 = PO7/PO5 assertion depends on PO5 (MAX6874)/PO3 (MAX6875) (Table 11). |
| | | [7] | 1 = PO7/PO5 assertion depends on PO6 (MAX6874)/PO4 (MAX6875) (Table 12). |
| 35h | 8035h | [0] | 1 = PO7 (MAX6874 only) assertion depends on PO8 (Table 14). Must be set to 0 for the MAX6875. |
| 40h | 8040h | [6] | 1 = PO7 asserts when \overline{MR} = low (Table 6). |

Table 13 only applies to PO7 of the MAX6874 and PO5 of the MAX6875. Write a 0 to a bit to make the PO7/PO5 output independent of the respective signal (IN_

thresholds, WD, GPI1–GPI4, \overline{MR} , or other programmable outputs).

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Table 14. PO8 (MAX6874 only) Output Dependency

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT | OUTPUT ASSERTION CONDITIONS |
|------------------|-----------------------|-------|--|
| 36h | 8036h | [0] | 1 = PO8 assertion depends on IN1 undervoltage threshold (Table 2). |
| | | [1] | 1 = PO8 assertion depends on IN2 undervoltage threshold (Table 3). |
| | | [2] | 1 = PO8 assertion depends on IN3 undervoltage threshold (Table 4). |
| | | [3] | 1 = PO8 assertion depends on IN4 undervoltage threshold (Table 4). |
| | | [4] | 1 = PO8 assertion depends on IN5 undervoltage threshold (Table 4). |
| | | [5] | 1 = PO8 assertion depends on IN6 undervoltage threshold (Table 4). |
| | | [6] | 1 = PO8 assertion depends on watchdog (Tables 18 and 19). |
| | | [7] | Must set to 0. |
| 37h | 8037h | [5:0] | Must set to 0. |
| | | [6] | 1 = PO8 assertion depends on GPI1 (Table 5). |
| | | [7] | 1 = PO8 assertion depends on GPI2 (Table 5). |
| 38h | 8038h | [0] | 1 = PO8 assertion depends on GPI3 (Table 5). |
| | | [1] | 1 = PO8 assertion depends on GPI4 (Table 5). |
| | | [2] | 1 = PO8 assertion depends on PO1 (Table 7). |
| | | [3] | 1 = PO8 assertion depends on PO2 (Table 8). |
| | | [4] | 1 = PO8 assertion depends on PO3 (Table 9). |
| | | [5] | 1 = PO8 assertion depends on PO4 (Table 10). |
| | | [6] | 1 = PO8 assertion depends on PO5 (Table 11). |
| | | [7] | 1 = PO8 assertion depends on PO6 (Table 12). |
| 39h | 8039h | [0] | 1 = PO8 assertion depends on PO7 (Table 13). |
| 40h | 8040h | [7] | 1 = PO8 asserts when MR = low (Table 6). |

Table 14 only applies to PO8 of the MAX6874. Write a 0 to a bit to make the PO8 output independent of the respective signal (IN1–IN6 thresholds, WD, GPI1–GPI4, MR, or other programmable outputs).

Output Stage Configurations

Independently program each programmable output as active-high or active-low (Table 15). All programmable outputs of the MAX6874/MAX6875 are open-drain only. See Table 16 to set the timeout period for each output.

Open-Drain Output Configuration

Connect an external pullup resistor from the programmable output to an external voltage when configured as an open-drain output. PO1–PO4 (PO1 and PO2 for the

MAX6875) may be pulled up to +13.2V. PO5–PO8 (PO3–PO5 for the MAX6875) may be pulled up to a voltage less than or equal to ABP. Choose the pullup resistor depending on the number of devices connected to the open-drain output and the allowable current consumption. The open-drain output configuration allows wire-ORed connections, and provides flexibility in setting the pullup current.

Configuring the MAX6874/MAX6875

The MAX6874/MAX6875 factory-default configuration sets all EEPROM registers to 00h except register 3Ah, which is set to FFh. This configuration sets all of the programmable outputs as active-high (putting all outputs into high-impedance states until the device is reconfig-

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Table 15. Programmable Output Active States

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | DESCRIPTION |
|------------------|-----------------------|-----------|---|
| 3Ah | 803Ah | [0] | PO1 (MAX6874 only). 0 = active low, 1 = active high. |
| | | [1] | PO2 (MAX6874 only). 0 = active low, 1 = active high. |
| | | [2] | PO3 (MAX6874)/PO1 (MAX6875). 0 = active low, 1 = active high. |
| | | [3] | PO4 (MAX6874)/PO2 (MAX6875). 0 = active low, 1 = active high. |
| | | [4] | PO5 (MAX6874)/PO3 (MAX6875). 0 = active low, 1 = active high. |
| | | [5] | PO6 (MAX6874)/PO4 (MAX6875). 0 = active low, 1 = active high. |
| | | [6] | PO7 (MAX6874)/PO5 (MAX6875). 0 = active low, 1 = active high. |
| | | [7] | PO8 (MAX6874 only). 0 = active low, 1 = active high. |

Table 16. PO_ Timeout Periods

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | AFFECTED OUTPUTS | | DESCRIPTION |
|------------------|-----------------------|-----------|------------------|---------|--|
| | | | MAX6874 | MAX6875 | |
| 11h | 8011h | [3:1] | PO1 | — | 000 = 25µs 001 = 1.5625ms 010 = 6.25ms 011 = 25ms 100 = 50ms 101 = 200ms 110 = 400ms 111 = 1600ms |
| 15h | 8015h | [3:1] | PO2 | — | |
| 1Ch | 801Ch | [4:2] | PO3 | PO1 | |
| 23h | 8023h | [4:2] | PO4 | PO2 | |
| 2Ah | 802Ah | [3:1] | PO5 | PO3 | |
| 31h | 8031h | [3:1] | PO6 | PO4 | |
| 35h | 8035h | [3:1] | PO7 | PO5 | |
| 39h | 8039h | [3:1] | PO8 | — | |

ured by the user). To configure the MAX6874/ MAX6875, first apply an input voltage to IN1 or one of IN3–IN5 (MAX6874)/IN3–IN4 (MAX6875) (see the *Powering the MAX6874/MAX6875* section). $V_{IN1} > +4V$ or one of $V_{IN3}–V_{IN5} > +2.7V$, to ensure device operation. Next, transmit data through the serial interface. Use the block write protocol to quickly configure the device. Write to the configuration registers first to ensure the device is configured properly. After completing the setup procedure, use the read word protocol to verify the data from the configuration registers. Lastly, use the write word protocol to write this data to the EEPROM registers. After completing EEPROM register configuration, apply full power to the system to begin normal operation. The non-volatile EEPROM stores the latest configuration upon removal of power. Write 0's to all EEPROM registers to clear the memory.

Software Reboot

A software reboot allows the user to restore the EEPROM configuration to the volatile registers without cycling the power supplies. Use the send byte command with data byte 88h to initiate a software reboot. The 3.5ms (max) power-up delay also applies after a software reboot.

SMBus/PC-Compatible Serial Interface

The MAX6874/MAX6875 feature an I²C/SMBus-compatible serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL allow bidirectional communication between the MAX6874/MAX6875 and the master device at clock rates up to 400kHz. Figure 2 shows the interface timing diagram. The MAX6874/MAX6875 are transmit/receive slave-only devices, relying upon a master device to generate a clock signal. The master device (typically a microcontroller) initiates data transfer on the bus and generates SCL to permit that transfer.

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A master device communicates to the MAX6874/MAX6875 by transmitting the proper address followed by command and/or data words. Each transmit sequence is framed by a START (S) or REPEATED START (SR) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse.

SCL is a logic input, while SDA is a logic input/open-drain output. SCL and SDA both require external pullup resistors to generate the logic-high voltage. Use 4.7kΩ for most applications.

Bit Transfer

Each clock pulse transfers one data bit. The data on SDA must remain stable while SCL is high (Figure 3), otherwise the MAX6874/MAX6875 register a START or STOP condition (Figure 4) from the master. SDA and SCL idle high when the bus is not busy.

Start and Stop Conditions

Both SCL and SDA idle high when the bus is not busy. A master device signals the beginning of a transmission with a START (S) condition (Figure 4) by transitioning SDA from high to low while SCL is high. The master device issues a STOP (P) condition (Figure 4) by transitioning SDA from low to high while SCL is high. A STOP condition frees the bus for another transmission. The bus remains active if a REPEATED START condition is generated, such as in the block read protocol (see Figure 7).

Early STOP Conditions

The MAX6874/MAX6875 recognize a STOP condition at any point during transmission except if a STOP condition occurs in the same high pulse as a START condition. This condition is not a legal I²C format. At least one clock pulse must separate any START and STOP condition.

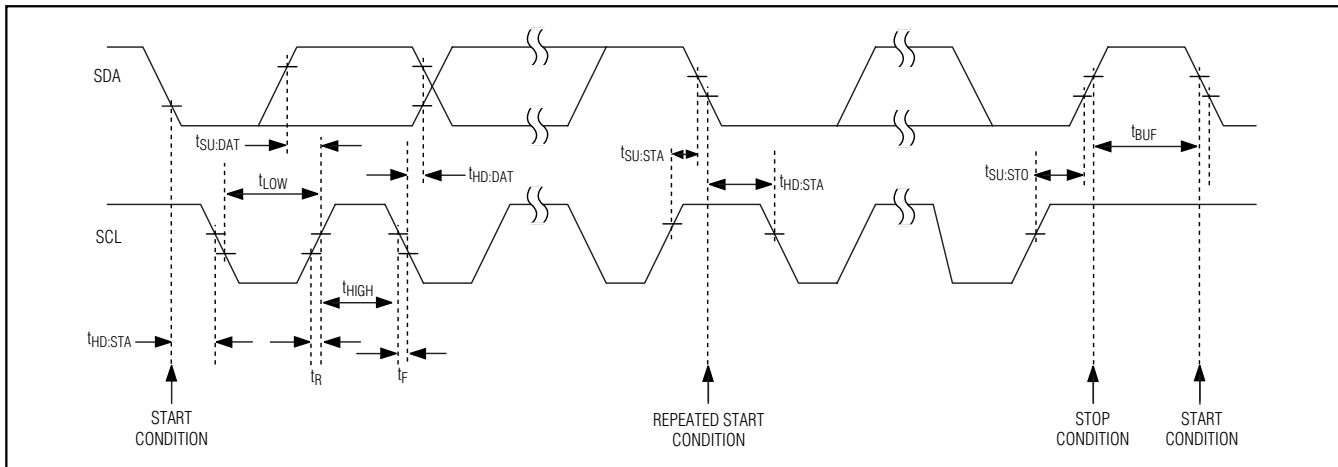


Figure 2. Serial-Interface Timing Details

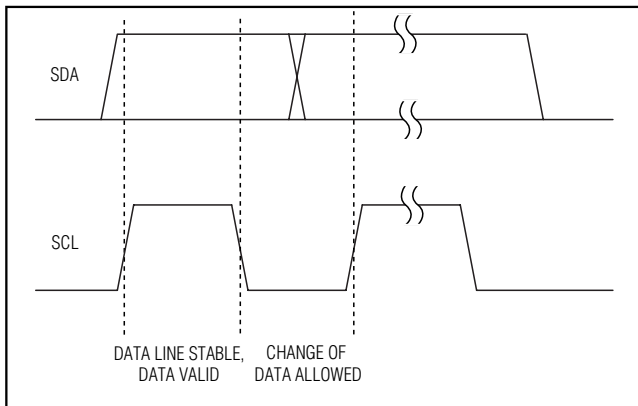


Figure 3. Bit Transfer

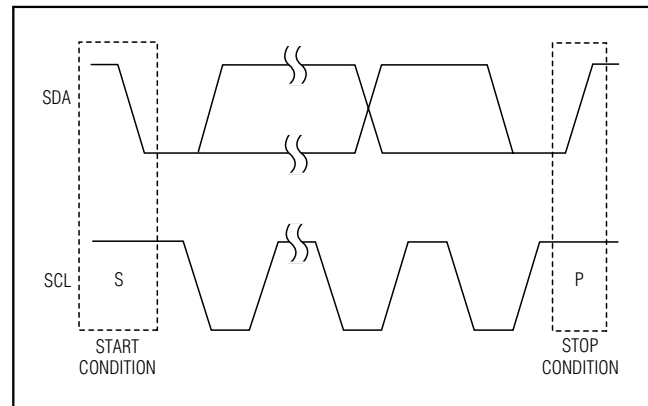


Figure 4. Start and Stop Conditions

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Repeated START Conditions

A REPEATED START (SR) condition may indicate a change of data direction on the bus. Such a change occurs when a command word is required to initiate a read operation (see Figure 7). SR may also be used when the bus master is writing to several I²C devices and does not want to relinquish control of the bus. The MAX6874/MAX6875 serial interface supports continuous write operations with or without an SR condition separating them. Continuous read operations require SR conditions because of the change in direction of data flow.

Acknowledge

The acknowledge bit (ACK) is the 9th bit attached to any 8-bit data word. The receiving device always generates an ACK. The MAX6874/MAX6875 generate an ACK when receiving an address or data by pulling SDA low during the 9th clock period (Figure 5). When transmitting data, such as when the master device reads data back from the MAX6874/MAX6875, the MAX6874/MAX6875 wait for the master device to generate an ACK. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if the receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time. The MAX6874/MAX6875 generate a NACK after the slave address during a software reboot, while writing to the EEPROM, or when receiving an illegal memory address.

Slave Address

The MAX6874 slave address conforms to the following table:

| SA7 (MSB) | SA6 | SA5 | SA4 | SA3 | SA2 | SA1 | SA0 (LSB) |
|-----------|-----|-----|-----|-----|-----|-----|-----------|
| 1 | 0 | 1 | 0 | A1 | A0 | X | R/W |

X = Don't care.

The MAX6875 slave address conforms to the following table:

| SA7 (MSB) | SA6 | SA5 | SA4 | SA3 | SA2 | SA1 | SA0 (LSB) |
|-----------|-----|-----|-----|-----|-----|-----|-----------|
| 1 | 0 | 1 | 0 | 0 | A0 | X | R/W |

X = Don't care.

SA7 through SA4 represent the standard interface address (1010) for devices with EEPROM. SA3 and SA2 correspond to the A1 and A0 address inputs of the MAX6874/MAX6875 (hardwired as logic low or logic high). A1 is internally set to 0 for the MAX6875. SA0 is a read/write flag bit (0 = write, 1 = read).

The A0 and A1 address inputs allow up to four MAX6874s or two MAX6875s to connect to one bus. Connect A0 and A1 to GND or to the serial interface power supply (see Figure 6).

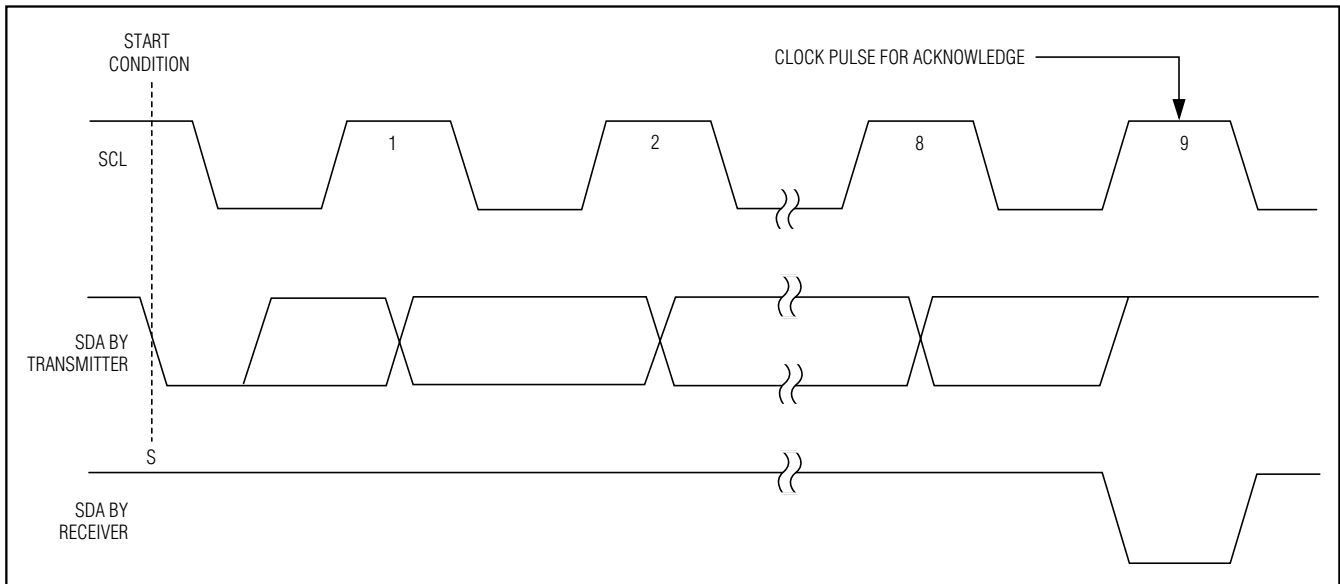


Figure 5. Acknowledge

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Send Byte

The send byte protocol allows the master device to send one byte of data to the slave device (see Figure 7). The send byte presets a register pointer address for a subsequent read or write. The slave sends a NACK instead of an ACK if the master tries to send an address that is not allowed. If the master sends 80h, 81h, or 82h, the data is ACK. This could be start of the write byte/word protocol, and the slave expects at least one further data byte. If the master sends a stop condition, the internal address pointer does not change. If the master sends 84h, this signifies that the block read protocol is expected, and a repeated start condition should follow. The device reboots if the master sends 88h. The send byte procedure follows:

- 1) The master sends a start condition.
- 2) The master sends the 7-bit slave address and a write bit (low).
- 3) The addressed slave asserts an ACK on SDA.
- 4) The master sends an 8-bit data byte.
- 5) The addressed slave asserts an ACK on SDA.
- 6) The master sends a stop condition.

Write Byte/Word

The write byte/word protocol allows the master device to write a single byte in the register bank, preset an EEPROM (configuration or user) address for a subsequent read, or to write a single byte to the configuration or user EEPROM (see Figure 7). The write byte/word procedure follows:

- 1) The master sends a start condition.

- 2) The master sends the 7-bit slave address and a write bit (low).
- 3) The addressed slave asserts an ACK on SDA.
- 4) The master sends an 8-bit command code.
- 5) The addressed slave asserts an ACK on SDA.
- 6) The master sends an 8-bit data byte.
- 7) The addressed slave asserts an ACK on SDA.
- 8) The master sends a stop condition or sends another 8-bit data byte.
- 9) The addressed slave asserts an ACK on SDA.
- 10) The master sends a stop condition.

To write a single byte to the register bank, only the 8-bit command code and a single 8-bit data byte are sent. The command code must be in the range of 00h to 45h. The data byte is written to the register bank if the command code is valid. The slave generates a NACK at step 5 if the command code is invalid.

To preset an EEPROM (configuration or user) address for a subsequent read, the 8-bit command code and a single 8-bit data byte are sent. The command code must be 80h if the write is to be directed into the configuration EEPROM, or 81h or 82h, if the write is to be directed into the user EEPROM. If the command code is 80h, the data byte must be in the range of 00h to 45h. If the command code is 81h or 82h, the data byte can be 00h to FFh. A NACK is generated in step 7 if none of the above conditions are true.

To write a single byte of data to the user or configuration EEPROM, the 8-bit command code and a single 8-bit data byte are sent. The following 8-bit data byte is written to the addressed EEPROM location.

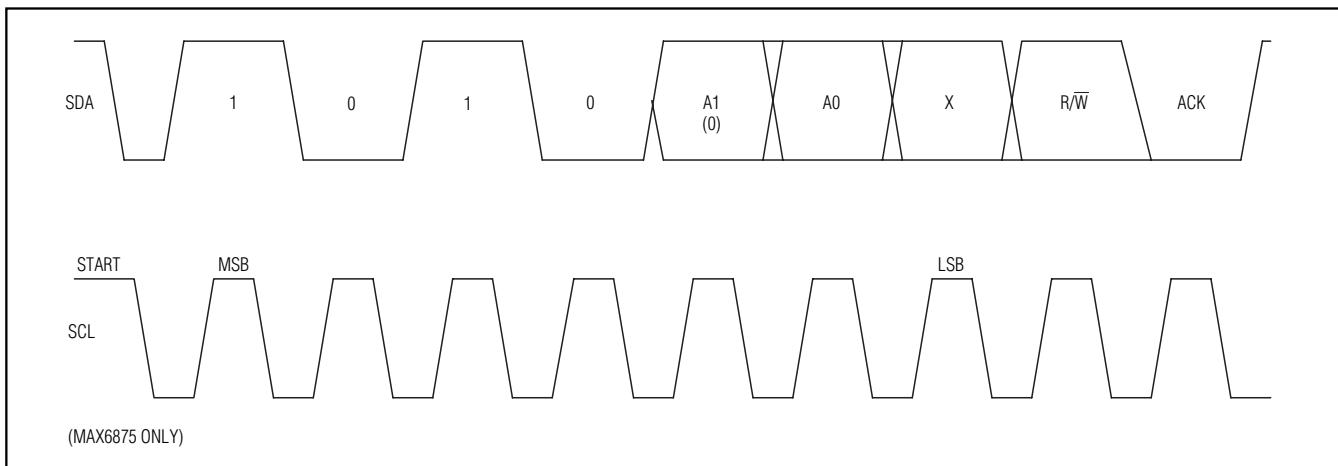


Figure 6. Slave Address

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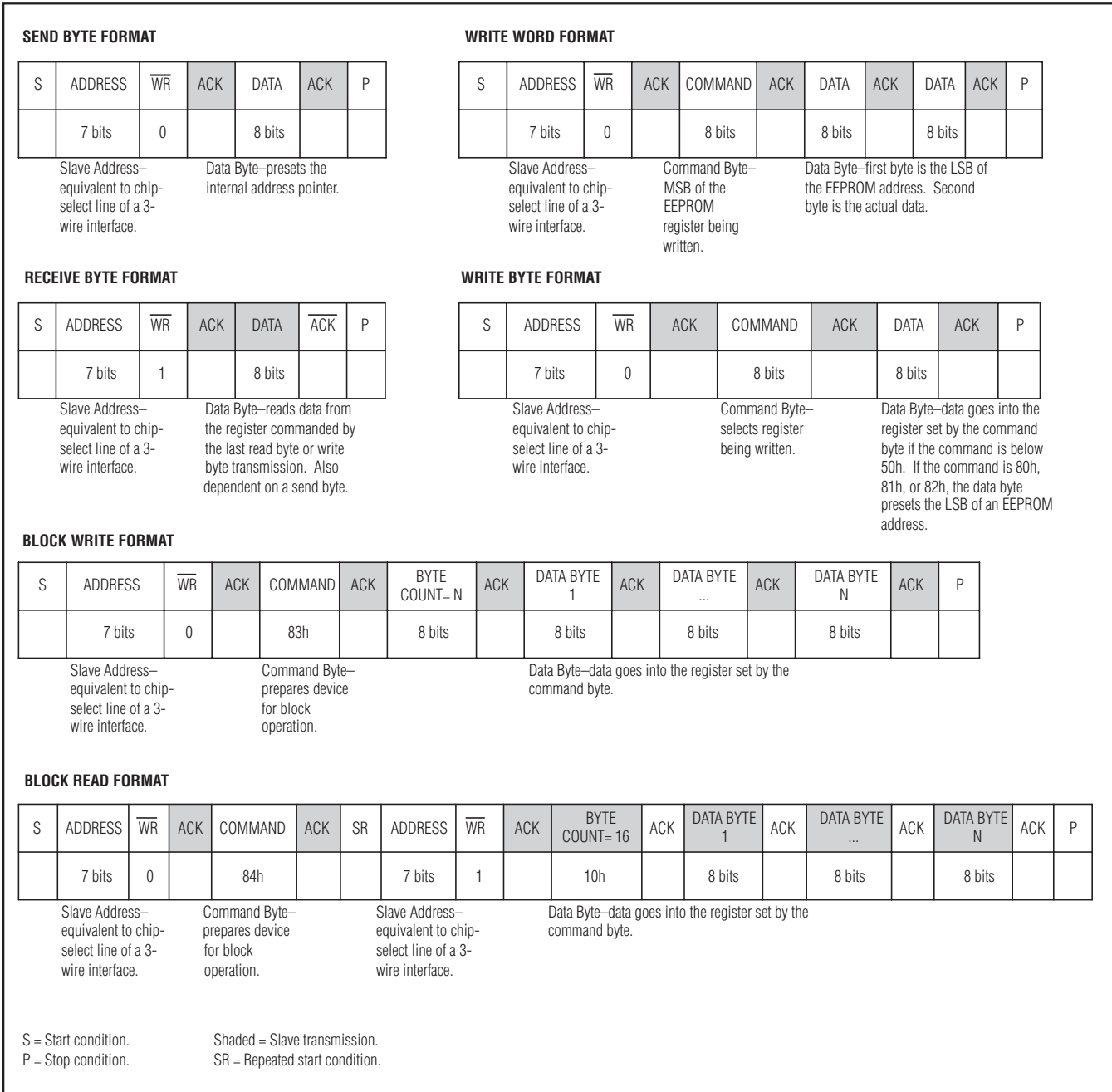


Figure 7. SMBus/I²C Protocols

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Block Write

The block write protocol allows the master device to write a block of data (1 to 16 bytes) to the EEPROM or to the register bank (see Figure 7). The destination address must already be set by the send byte or write byte protocol and the command code must be 83h. If the number of bytes to be written causes the address pointer to exceed 45h for the configuration register or configuration EEPROM, the address pointer stays at 45h, overwriting this memory address with the remaining bytes of data. The last data byte sent is stored at register address 45h. If the number of bytes to be written exceeds the address pointer FFh for the user EEPROM, the address pointer loops back to 00h, and continues writing bytes until all data is written. The block write procedure follows:

- 1) The master sends a start condition.
- 2) The master sends the 7-bit slave address and a write bit (low).
- 3) The addressed slave asserts an ACK on SDA.
- 4) The master sends the 8-bit command code for block write (83h).
- 5) The addressed slave asserts an ACK on SDA.
- 6) The master sends the 8-bit byte count (1 to 16 bytes) N.
- 7) The addressed slave asserts an ACK on SDA.
- 8) The master sends 8 bits of data.
- 9) The addressed slave asserts an ACK on SDA.
- 10) Repeat steps 8 and 9 one time.
- 11) The master generates a stop condition.

Receive Byte

The receive byte protocol allows the master device to read the register content of the MAX6874/MAX6875 (see Figure 7). The EEPROM or register address must be preset with a send byte or write word protocol first. Once the read is complete, the internal pointer increases by one. Repeating the receive byte protocol reads the contents of the next address. The receive byte procedure follows:

- 1) The master sends a start condition.
- 2) The master sends the 7-bit slave address and a read bit (high).
- 3) The addressed slave asserts an ACK on SDA.
- 4) The slave sends 8 data bits.

- 5) The master asserts a NACK on SDA.
- 6) The master generates a stop condition.

Block Read

The block read protocol allows the master device to read a block of 16 bytes from the EEPROM or register bank (see Figure 7). Read fewer than 16 bytes of data by issuing an early STOP condition from the master, or by generating a NACK with the master. The send byte or write byte protocol predetermines the destination address with a command code of 84h. The block read procedure follows:

- 1) The master sends a start condition.
- 2) The master sends the 7-bit slave address and a write bit (low).
- 3) The addressed slave asserts an ACK on SDA.
- 4) The master sends 8 bits of the block read command (84h).
- 5) The slave asserts an ACK on SDA, unless busy.
- 6) The master generates a repeated start condition.
- 7) The master sends the 7-bit slave address and a read bit (high).
- 8) The slave asserts an ACK on SDA.
- 9) The slave sends the 8-bit byte count (16).
- 10) The master asserts an ACK on SDA.
- 11) The slave sends 8 bits of data.
- 12) The master asserts an ACK on SDA.
- 13) Repeat steps 8 and 9 fifteen times.
- 14) The master generates a stop condition.

Address Pointers

Use the send byte protocol to set the register address pointers before read and write operations. For the configuration registers, valid address pointers range from 00h to 45h. Register addresses outside of this range result in a NACK being issued from the MAX6874/MAX6875. When using the block write protocol, the address pointer automatically increments after each data byte, except when the address pointer is already at 45h. If the address pointer is already 45h, and more data bytes are being sent, these subsequent bytes overwrite address 45h repeatedly, leaving only the last data byte sent stored at this register address.

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For the configuration EEPROM, valid address pointers range from 8000h to 8045h. Registers 8046h to 804Fh are reserved and should not be overwritten. Register addresses from 8050h to 80FFh return a NACK from the MAX6874/MAX6875. When using the block write protocol, the address pointer automatically increments after each data byte, except when the address pointer is already at 8045h. If the address pointer is already 8045h, and more data bytes are being sent, these subsequent bytes overwrite address 8045h repeatedly, leaving only the last data byte sent stored at this register address.

For the user EEPROM, valid address pointers range from 8100h to 81FFh and 8200h to 82FFh. Block write and block read protocols allow the address pointer to reset (to 8100h or 8200h) when attempting to write or read beyond 81FFh or 82FFh.

Configuration EEPROM

The configuration EEPROM addresses range from 8000h to 8045h. Write data to the configuration EEPROM to automatically set up the MAX6874/MAX6875 upon power-up. Data transfers from the configuration EEPROM to the configuration registers when ABP exceeds UVLO during power-up or after a software reboot. After ABP exceeds UVLO, an internal 1MHz clock starts after a 5 μ s delay, and data transfer begins. Data transfer disables access to the configuration registers and EEPROM. The data transfer from EEPROM to configuration registers takes 3.5ms (max). Read configuration EEPROM data at any

time after power-up or software reboot. Write commands to the configuration EEPROM are allowed at any time after power-up or software reboot, unless the configuration lock bit is set (see Table 20). The maximum cycle time to write a single byte is 11ms (max).

User EEPROM

The 512 byte user EEPROM addresses range from 8100h to 82FFh (see Figure 7). Store software-revision data, board-revision data, and other data in these registers. The maximum cycle time to write a single byte is 11ms (max).

Configuration Register Bank and EEPROM

The configuration registers can be directly modified by the serial interface without modifying the EEPROM after the power-up procedure terminates and the configuration EEPROM data has been loaded into the configuration register bank. Use the write byte or block write protocols to write directly to the configuration registers. Changes to the configuration registers take effect immediately and are lost upon power removal.

At device power-up, the register bank loads configuration data from the EEPROM. Configuration data may be directly altered in the register bank during application development, allowing maximum flexibility. Transfer the new configuration data, byte by byte, to the configuration EEPROM with the write byte protocol. The next device power-up or software reboot automatically loads the new configuration.

Table 17. Register Map

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | READ/ WRITE | DESCRIPTION |
|------------------|-----------------------|-------------|---|
| 00h | 8000h | R/W | IN1 undervoltage detector threshold (Table 2). |
| 01h | 8001h | R/W | IN2 undervoltage detector threshold (Table 3). |
| 02h | 8002h | R/W | IN3 undervoltage detector threshold (Table 4). |
| 03h | 8003h | R/W | IN4 undervoltage detector threshold (Table 4). |
| 04h | 8004h | R/W | IN5 undervoltage detector threshold (MAX6874 only) (Table 4). |
| 05h | 8005h | R/W | IN6 undervoltage detector threshold (MAX6874 only) (Table 4). |
| 06h | 8006h | — | Not used. |
| 07h | 8007h | — | Not used. |
| 08h | 8008h | — | Not used. |
| 09h | 8009h | — | Not used. |
| 0Ah | 800Ah | — | Not used. |

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MAX6874/MAX6875

Table 17. Register Map (continued)

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | READ/ WRITE | DESCRIPTION |
|------------------|-----------------------|-------------|---|
| 0Bh | 800Bh | — | Not used. |
| 0Ch | 800Ch | — | Not used. |
| 0Dh | 800Dh | R/W | Threshold range selection (Tables 2–4). |
| 0Eh | 800Eh | R/W | PO1 (MAX6874 only) input selection (Table 7). |
| 0Fh | 800Fh | R/W | PO1 (MAX6874 only) input selection (Table 7). |
| 10h | 8010h | R/W | PO1 (MAX6874 only) input selection (Table 7). |
| 11h | 8011h | R/W | PO1 (MAX6874 only) input selection, PO_ timeout period, and output type selection (Tables 7, 16). |
| 12h | 8012h | R/W | PO2 (MAX6874 only) input selection (Table 8). |
| 13h | 8013h | R/W | PO2 (MAX6874 only) input selection (Table 8). |
| 14h | 8014h | R/W | PO2 (MAX6874 only) input selection (Table 8). |
| 15h | 8015h | R/W | PO2 (MAX6874 only) input selection and PO_ timeout period (Tables 8, 16). |
| 16h | 8016h | R/W | PO3 (MAX6874)/PO1 (MAX6875) input selection (Table 9). |
| 17h | 8017h | R/W | PO3 (MAX6874)/PO1 (MAX6875) input selection (Table 9). |
| 18h | 8018h | R/W | PO3 (MAX6874)/PO1 (MAX6875) input selection (Table 9). |
| 19h | 8019h | R/W | Set to 0. |
| 1Ah | 801Ah | R/W | Set to 0. |
| 1Bh | 801Bh | R/W | Set to 0. |
| 1Ch | 801Ch | R/W | PO3 (MAX6874)/PO1 (MAX6875) input selection and PO_ timeout period (Tables 9, 16). |
| 1Dh | 801Dh | R/W | PO4 (MAX6874)/PO2 (MAX6875) input selection (Table 10). |
| 1Eh | 801Eh | R/W | PO4 (MAX6874)/PO2 (MAX6875) input selection (Table 10). |
| 1Fh | 801Fh | R/W | PO4 (MAX6874)/PO2 (MAX6875) input selection (Table 10). |
| 20h | 8020h | R/W | Set to 0. |
| 21h | 8021h | R/W | Set to 0. |
| 22h | 8022h | R/W | Set to 0. |
| 23h | 8023h | R/W | PO4 (MAX6874)/PO2 (MAX6875) input selection and PO_ timeout period (Tables 6, 18). |
| 24h | 8024h | R/W | PO5 (MAX6874)/PO3 (MAX6875) input selection (Table 11). |
| 25h | 8025h | R/W | PO5 (MAX6874)/PO3 (MAX6875) input selection (Table 11). |
| 26h | 8026h | R/W | PO5 (MAX6874)/PO3 (MAX6875) input selection (Table 11). |
| 27h | 8027h | R/W | Set to 0. |
| 28h | 8028h | R/W | Set to 0. |
| 29h | 8029h | R/W | Set to 0. |
| 2Ah | 802Ah | R/W | PO5 (MAX6874)/PO3 (MAX6875) input selection and PO_ timeout period (Tables 11, 18). |
| 2Bh | 802Bh | R/W | PO6 (MAX6874)/PO4 (MAX6875) input selection (Table 12). |
| 2Ch | 802Ch | R/W | PO6 (MAX6874)/PO4 (MAX6875) input selection (Table 12). |

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Table 17. Register Map (continued)

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | READ/ WRITE | DESCRIPTION |
|------------------|-----------------------|-------------|---|
| 2Dh | 802Dh | R/W | PO6 (MAX6874)/PO4 (MAX6875) input selection (Table 12). |
| 2Eh | 802Eh | R/W | Set to 0. |
| 2Fh | 802Fh | R/W | Set to 0. |
| 30h | 8030h | R/W | Set to 0. |
| 31h | 8031h | R/W | PO6 (MAX6874)/PO4 (MAX6875) input selection and PO_ reset timeout period (Tables 12, 16). |
| 32h | 8032h | R/W | PO7 (MAX6874)/PO5 (MAX6875) input selection (Table 13). |
| 33h | 8033h | R/W | PO7 (MAX6874)/PO5 (MAX6875) input selection (Table 13). |
| 34h | 8034h | R/W | PO7 (MAX6874)/PO5 (MAX6875) input selection (Table 13). |
| 35h | 8035h | R/W | PO7 (MAX6874)/PO5 (MAX6875) input selection and PO_ timeout period (Tables 13, 16). |
| 36h | 8036h | R/W | PO8 (MAX6874 only) input selection (Table 14). |
| 37h | 8037h | R/W | PO8 (MAX6874 only) input selection (Table 14). |
| 38h | 8038h | R/W | PO8 (MAX6874 only) input selection (Table 14). |
| 39h | 8039h | R/W | PO8 (MAX6874 only) input selection and PO_ timeout period (Tables 14, 16). |
| 3Ah | 803Ah | R/W | Programmable output polarity (active high/active low) (Table 15). |
| 3Bh | 803Bh | R/W | GPI_ input polarity, PO5, PO6 (Table 5). |
| 3Ch | 803Ch | R/W | WD input selection and timeout enable (Table 18). |
| 3Dh | 803Dh | R/W | WD initial and normal timeout duration (Table 19). |
| 3Eh | 803Eh | R/W | Must be set to 0. |
| 3Fh | 803Fh | R/W | Must be set to 0. |
| 40h | 8040h | R/W | \overline{MR} input and programmable output behavior (Table 6). |
| 41h | 8041h | R/W | Must be set to 0. |
| 42h | 8042h | R/W | Must be set to 0. |
| 43h | 8043h | R/W | User EEPROM write disable (Table 21). |
| 44h | 8044h | — | Reserved. Should not be overwritten. |
| 45h | 8045h | R/W | Configuration lock (Table 20). |

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MAX6874/MAX6875

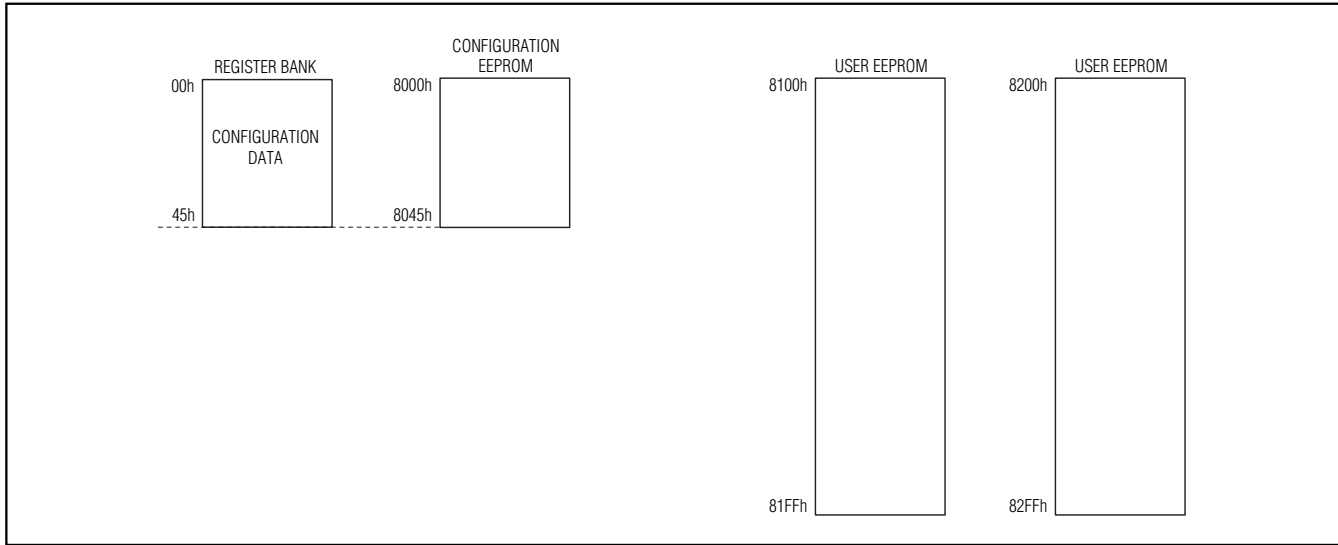


Figure 8. Memory Map

Table 18. Watchdog Inputs

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | DESCRIPTION |
|------------------|-----------------------|-----------|---|
| 3Ch | 803Ch | [1:0] | Watchdog Input Selection: 00 = GPI1 01 = GPI2 10 = GPI3 11 = GPI4 (MAX6874 only) |
| | | [4:2] | Watchdog Internal Input Selection: 000 = PO1 (MAX6874), not used (MAX6875) 001 = PO2 (MAX6874), not used (MAX6875) 010 = PO3 (MAX6874), PO1 (MAX6875) 011 = PO4 (MAX6874), PO2 (MAX6875) 100 = PO5 (MAX6874), PO3 (MAX6875) 101 = PO6 (MAX6874), PO4 (MAX6875) 110 = PO7 (MAX6874), PO5 (MAX6875) 111 = PO8 (MAX6874), not used (MAX6875) |
| | | [6:5] | Watchdog Dependency on Inputs: 00 = 11 = Watchdog clear depends on both GPI_ from 3Ch[1:0] and PO_ from 3Ch[4:2]. 01 = Watchdog clear depends only on PO_ from 3Ch[4:2]. 10 = Watchdog clear depends only on GPI_ from 3Ch[1:0]. |
| | | [7] | Must be set to 1 |

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Table 19. Watchdog Timeout Period Selection

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | DESCRIPTION |
|------------------|-----------------------|-----------|---|
| 3Dh | 803Dh | [2:0] | Normal Watchdog Timeout Period: 000 = 6.25ms 001 = 25ms 010 = 100ms 011 = 400ms 100 = 1.6s 101 = 6.4s 110 = 25.6s 111 = 102.4s |
| | | [5:3] | Initial Watchdog Timeout Period (immediately following power-up, reset event, or enabling watchdog): 000 = 6.25ms 001 = 25ms 010 = 100ms 011 = 400ms 100 = 1.6s 101 = 6.4s 110 = 25.6s 111 = 102.4s |
| | | [6] | Watchdog Enable: 0 = Disables watchdog timer 1 = Enables watchdog timer |
| | | [7] | Not used |

Configuring the Watchdog Timer (Registers 3Ch–3Dh)

A watchdog timer monitors microprocessor (μ P) software execution for a stalled condition and resets the μ P if it stalls. The output of a watchdog timer (one of the programmable outputs) connects to the reset input or a nonmaskable interrupt of the μ P.

Registers 3Ch–3Dh configure the watchdog functionality of the MAX6874/MAX6875. Program the watchdog timer to assert one or more programmable outputs (see Tables 7–14). Program the watchdog timer to reset on one of the GPI_ inputs, one of the programmable outputs, or a combination of one GPI_ input and one programmable output.

The watchdog timer features independent initial and normal watchdog timeout periods. The initial watchdog timeout period applies immediately after power-up, after a reset event takes place, or after enabling the watchdog timer. The initial watchdog timeout period allows the μ P to perform its initialization process. If no pulse occurs during the initial watchdog timeout period, the μ P is taking too long to initialize, indicating a potential problem.

The normal watchdog timeout period applies in every other cycle after the initial watchdog timeout period occurs. The normal watchdog timeout period monitors a pulsed output of the μ P that indicates when normal processor behavior occurs. If no pulse occurs during the normal watchdog timeout period, this indicates that the processor has stopped operating or is stuck in an infinite execution loop.

Register 3Dh programs the initial and normal watchdog timeout periods, and enables or disables the watchdog timer. See Tables 18 and 19 for a summary of the watchdog behavior.

Configuration Lock

Lock the configuration register bank and configuration EEPROM contents after initial programming by setting the lock bit high (see Table 20). Locking the configuration prevents write operations to all registers except the configuration lock register. Clear the lock bit to reconfigure the device.

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Table 20. Configuration Lock Register

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | DESCRIPTION |
|------------------|-----------------------|-----------|--|
| 45h | 8045h | [0] | 0 = configuration unlocked. 1 = configuration locked. |
| | | [7:1] | Not used. |

Table 21. Write Disable Register

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | DESCRIPTION |
|------------------|-----------------------|-----------|--|
| 43h | 8043h | [0] | 0 = write not disabled if PO1 asserts (MAX6874). 1 = write disabled if PO1 asserts (MAX6874). Set to 0 (MAX6875). |
| | | [1] | 0 = write not disabled if PO2 asserts (MAX6874). 1 = write disabled if PO2 asserts (MAX6874). Set to 0 (MAX6875). |
| | | [2] | 0 = write not disabled if PO3 (MAX6874)/PO1 (MAX6875) asserts. 1 = write disabled if PO3 (MAX6874)/PO1 (MAX6875) asserts. |
| | | [3] | 0 = write not disabled if PO4 (MAX6874)/PO2 (MAX6875) asserts. 1 = write disabled if PO4 (MAX6874)/PO2 (MAX6875) asserts. |
| | | [4] | 0 = write not disabled if PO5 (MAX6874)/PO3 (MAX6875) asserts. 1 = write disabled if PO5 (MAX6874)/PO3 (MAX6875) asserts. |
| | | [5] | 0 = write not disabled if PO6 (MAX6874)/PO4 (MAX6875) asserts. 1 = write disabled if PO6 (MAX6874)/PO4 (MAX6875) asserts. |
| | | [6] | 0 = write not disabled if PO7 (MAX6874)/PO5 (MAX6875) asserts. 1 = write disabled if PO7 (MAX6874)/PO5 (MAX6875) asserts. |
| | | [7] | 0 = write not disabled if PO8 asserts (MAX6874). 1 = write disabled if PO8 asserts (MAX6874). Set to 0 (MAX6875). |

Write Disable

A unique write disable feature protects the MAX6874/MAX6875 from inadvertent user EEPROM writes. As input voltages that power the serial interface, a μ P, or any other writing devices fall, unintentional data may be written onto the data bus. The user EEPROM write disable function (see Table 21) ensures that unintentional data does not corrupt the MAX6874/MAX6875 EEPROM data.

Applications Information

Configuration Download at Power-up

The configuration of the MAX6874/MAX6875 (under-voltage thresholds, PO_ timeout periods, watchdog behavior, programmable output conditions, etc.) depends on the contents of the EEPROM. The EEPROM is comprised of buffered latches that store the configura-

tion. The local volatile memory latches lose their contents at power-down. Therefore, at power-up, the device configuration must be restored by downloading the contents of the EEPROM (non-volatile memory) to the local latches. This download occurs in a number of steps:

- 1) Programmable outputs go high impedance with no power applied to the device.
- 2) When ABP exceeds +1V, all programmable outputs are weakly pulled to GND through a 10 μ A current sink.
- 3) When ABP exceeds UVLO, the configuration EEPROM starts to download its contents to the volatile configuration registers. The programmable outputs assume their programmed conditional output state when download is complete.

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- 4) Any attempt to communicate with the device prior to this download completion results in a NACK being issued from the MAX6874/MAX6875.

Forcing Programmable Outputs High During Power-Up

A weak 10 μ A pulldown holds all programmable outputs low during power-up until ABP exceeds the undervoltage lockout (UVLO) threshold. Applications requiring a guaranteed high programmable output for ABP down to GND require external pullup resistors to maintain the logic state until ABP exceeds UVLO. Use 20k Ω resistors for most applications.

Uses for General-Purpose Inputs (GPI1–GPI4)

Watchdog Timer

Program GPI_n as an input to the watchdog timer in the MAX6874/MAX6875. The GPI_n input must toggle within the watchdog timeout period, otherwise any programmable output dependent on the watchdog timer asserts.

Additional Manual Reset Functions

Program PO7 (MAX6874)/PO5 (MAX6875) to depend on one of the GPI_n inputs. Any output that depends on GPI_n asserts when GPI_n is held in its active state, effectively acting as a manual reset input.

Other Fault Signals from μ C

Connect a general-purpose output from a μ C to one of the GPI_n inputs to allow interrupts to assert any output of the MAX6874/MAX6875. Configure one of the programmable outputs to assert on whichever GPI_n input connects to the general purpose output of the μ C.

Layout and Bypassing

For better noise immunity, bypass each of the voltage detector inputs to GND with 0.1 μ F capacitors installed as close to the device as possible. Bypass ABP and DBP to GND with 1 μ F capacitors installed as close to the device as possible. ABP and DBP are internally generated voltages and should not be used to supply power to external circuitry.

Configuration Latency Period

A delay of less than 5 μ s occurs between writing to the configuration registers and the time when these changes actually take place, except when changing one of the voltage-detector thresholds. Changing a voltage-detector threshold typically takes 150 μ s. When changing EEPROM contents, a software reboot or cycling of power is required for these changes to transfer to volatile memory.

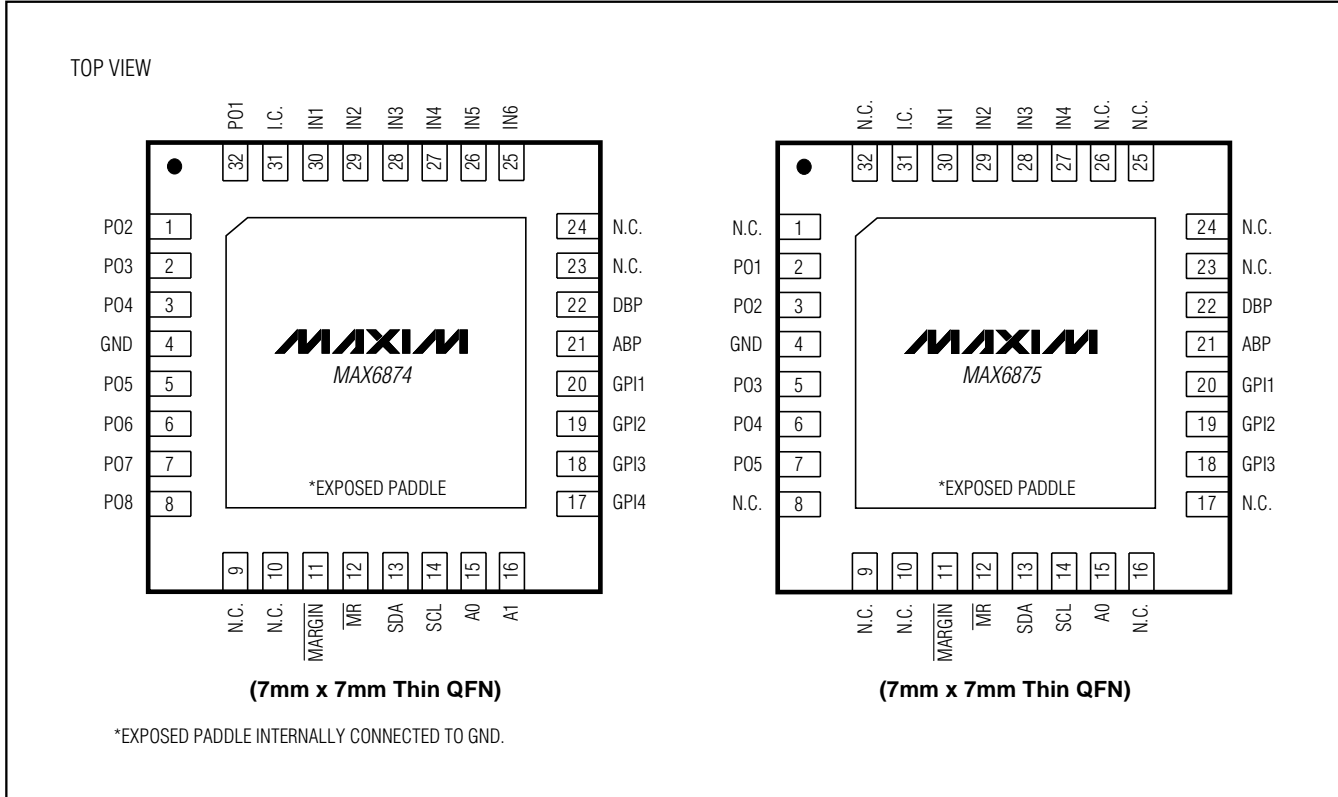
Chip Information

PROCESS: BiCMOS

EEPROM-Programmable, Hex/Quad, Power-Supply Sequencers/Supervisors

Pin Configurations

MAX6874/MAX6875

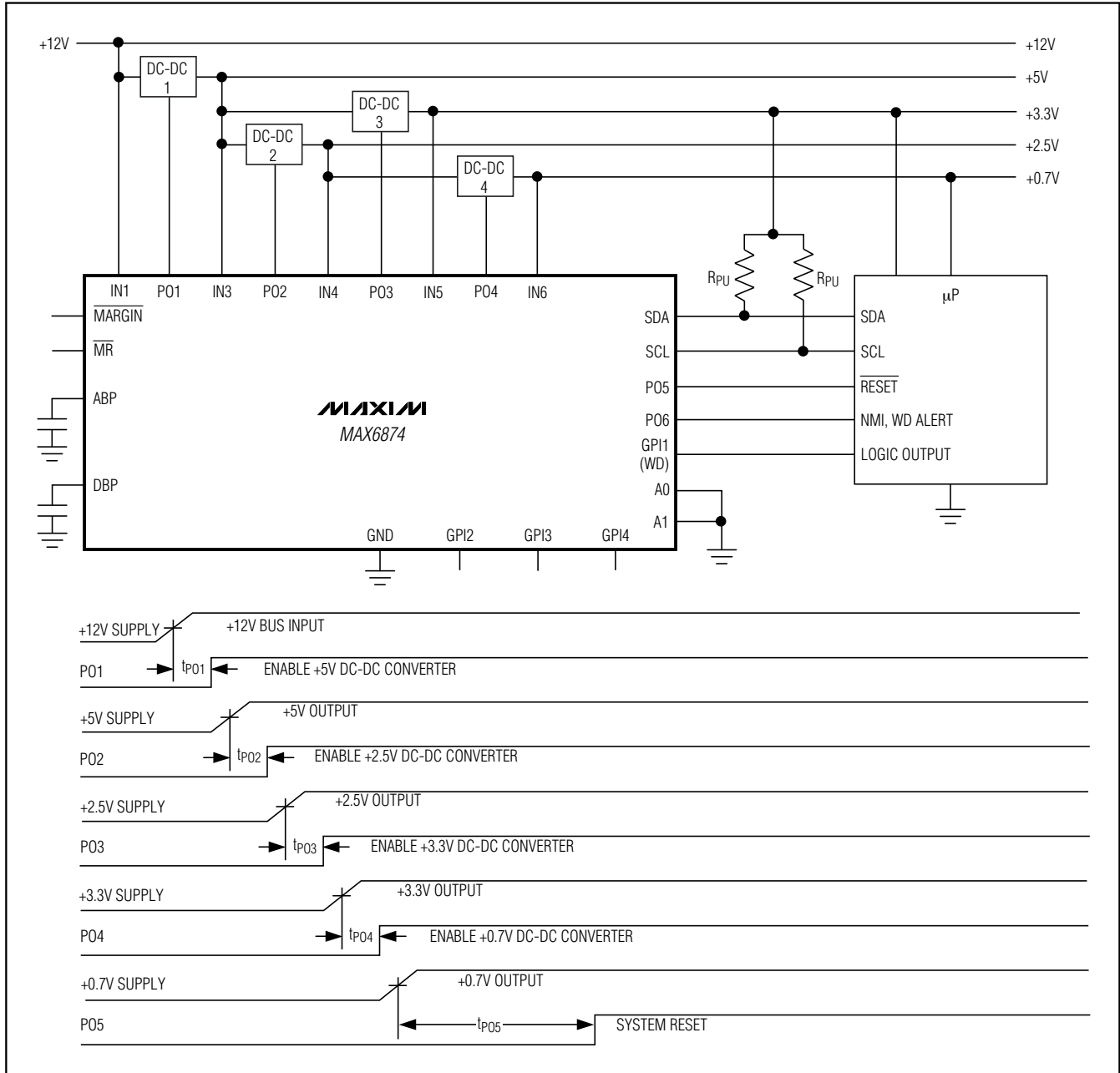


Selector Guide

| PART | VOLTAGE-DETECTOR INPUTS | GENERAL-PURPOSE INPUTS | PROGRAMMABLE OUTPUTS |
|------------|-------------------------|------------------------|----------------------|
| MAX6874ETJ | 6 | 4 | 8 |
| MAX6875ETJ | 4 | 3 | 5 |

EEPROM-Programmable, Hex/Quad, Power-Supply Sequencers/Supervisors

Typical Operating Circuit



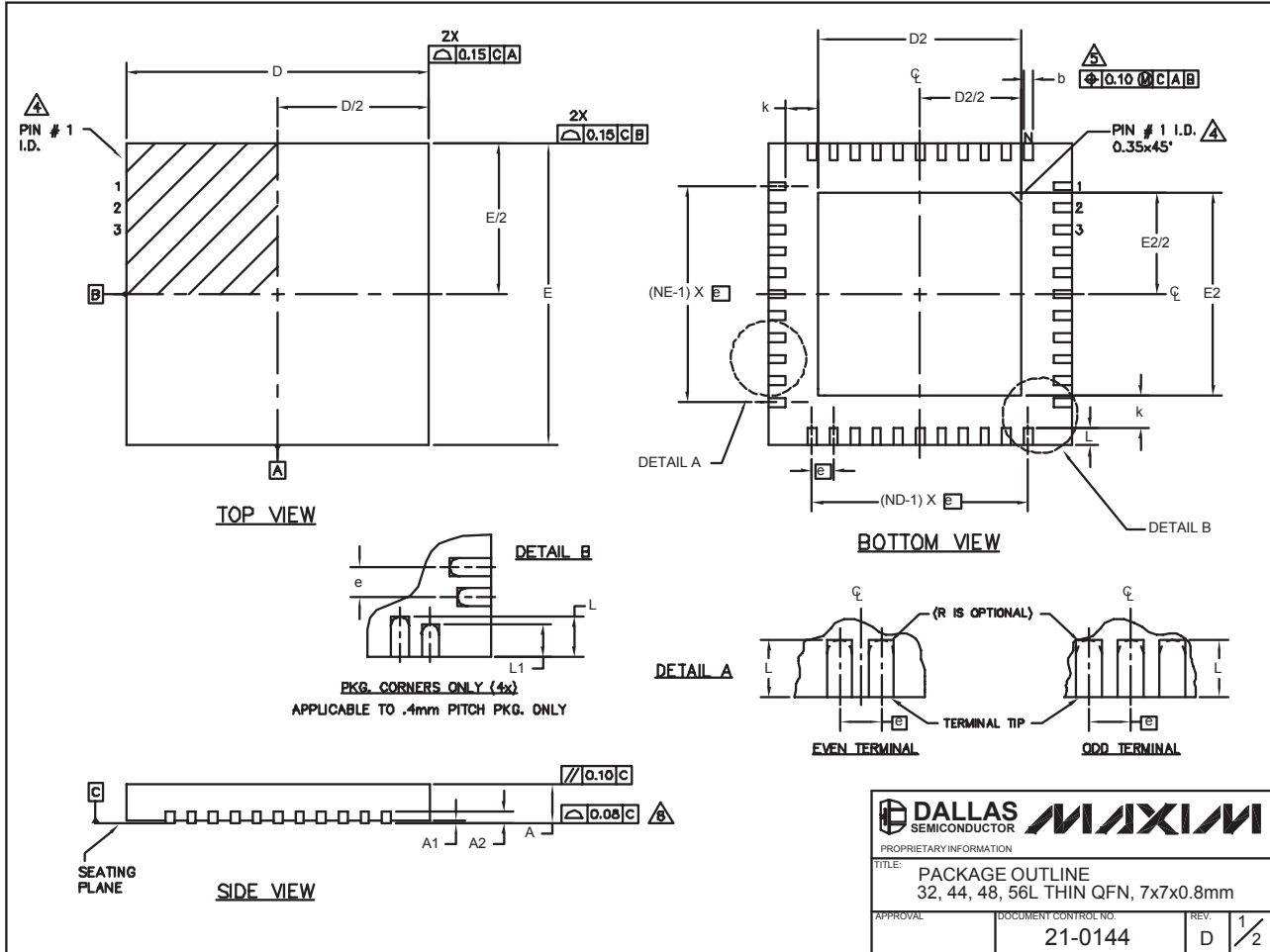
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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX6874/MAX6875

32, 44, 48L QFN.EPS



EEPROM-Programmable, Hex/Quad, Power-Supply Sequencers/Supervisors

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

| COMMON DIMENSIONS | | | | | | | | | | | | | | | |
|-------------------|-----------|------|------|-----------|------|------|-----------|------|------|-------------------------------------|------|------|-----------|------|------|
| PKG | 32L 7x7 | | | 44L 7x7 | | | 48L 7x7 | | | CUSTOM PKG. (T4877-1) 48L 7x7 | | | 56L 7x7 | | |
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| SYMBOL | | | | | | | | | | | | | | | |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | - | 0.05 |
| A2 | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | |
| b | 0.25 | 0.30 | 0.35 | 0.20 | 0.25 | 0.30 | 0.20 | 0.25 | 0.30 | 0.20 | 0.25 | 0.30 | 0.15 | 0.20 | 0.25 |
| D | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 |
| E | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 |
| e | 0.65 BSC. | | | 0.50 BSC. | | | 0.50 BSC. | | | 0.50 BSC. | | | 0.40 BSC. | | |
| k | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | 0.35 | 0.45 |
| L | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 | 0.45 | 0.55 | 0.65 | 0.40 | 0.50 | 0.60 |
| L1 | - | - | - | - | - | - | - | - | - | - | - | - | 0.30 | 0.40 | 0.50 |
| N | 32 | | | 44 | | | 48 | | | 44 | | | 56 | | |
| ND | 8 | | | 11 | | | 12 | | | 10 | | | 14 | | |
| NE | 8 | | | 11 | | | 12 | | | 12 | | | 14 | | |

| EXPOSED PAD VARIATIONS | | | | | | | | | |
|------------------------|-------------------|------|------|------|------|------|------|--------------------|--------------------|
| PKG. CODES | DEPOPULATED LEADS | D2 | | | E2 | | | JEDEC MO220 REV. C | DOWN BONDS ALLOWED |
| | | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | | |
| T3277-1 | - | 4.55 | 4.70 | 4.85 | 4.55 | 4.70 | 4.85 | - | NO |
| T3277-2 | - | 4.55 | 4.70 | 4.85 | 4.55 | 4.70 | 4.85 | - | YES |
| T4477-1 | - | 4.55 | 4.70 | 4.85 | 4.55 | 4.70 | 4.85 | WKD-1 | NO |
| T4477-2 | - | 4.55 | 4.70 | 4.85 | 4.55 | 4.70 | 4.85 | WKD-1 | YES |
| T4477-3 | - | 4.55 | 4.70 | 4.85 | 4.55 | 4.70 | 4.85 | WKD-1 | YES |
| T4877-1** | 13,24,37,48 | 4.20 | 4.30 | 4.40 | 4.20 | 4.30 | 4.40 | - | NO |
| T4877-2 | - | 5.45 | 5.60 | 5.63 | 5.45 | 5.60 | 5.63 | - | NO |
| T4877-3 | - | 4.95 | 5.10 | 5.25 | 4.95 | 5.10 | 5.25 | - | YES |
| T4877-4 | - | 5.45 | 5.60 | 5.63 | 5.45 | 5.60 | 5.63 | - | YES |
| T4877-5 | - | 2.40 | 2.50 | 2.60 | 2.40 | 2.50 | 2.60 | - | NO |
| T4877-6 | - | 5.45 | 5.60 | 5.63 | 5.45 | 5.60 | 5.63 | - | NO |
| T5677-1 | - | 5.20 | 5.30 | 5.40 | 5.20 | 5.30 | 5.40 | - | YES |

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220 EXCEPT THE EXPOSED PAD DIMENSIONS OF T3277-1; T4877-1/-2/-3/-4/-5/-6 & T5677-1.
- WARPAGE SHALL NOT EXCEED 0.10 mm.

| | |
|--|--|
| | |
| <small>PROPRIETARY INFORMATION</small> | |
| TITLE: PACKAGE OUTLINE 32, 44, 48, 56L THIN QFN, 7x7x0.8mm | |
| <small>APPROVAL</small> | <small>DOCUMENT CONTROL NO.</small> 21-0144 |
| <small>REV.</small> D | <small>2/2</small> |

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